NEHRU COLLEGE OF ENGINEERING AND RESEARCH CENTRE
(NAAC Accredited)
(Approved by AICTE, Affiliated to APJ Abdul Kalam Technological University, Kerala)

DEPARTMENT OF MECHATRONICS ENGINEERING

COURSE MATERIALS

EC 209 ANALOG ELECTRONICS

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2013
- Course offered: B.Tech Mechatronics Engineering
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

DEPARTMENT VISION

To develop professionally ethical and socially responsible Mechatronics engineers to serve the humanity through quality professional education.

DEPARTMENT MISSION

1) The department is committed to impart the right blend of knowledge and quality education to create professionally ethical and socially responsible graduates.

2) The department is committed to impart the awareness to meet the current challenges in technology.

3) Establish state-of-the-art laboratories to promote practical knowledge of mechatronics to meet the needs of the society

PROGRAMME EDUCATIONAL OBJECTIVES

I. Graduates shall have the ability to work in multidisciplinary environment with good professional and commitment.

II. Graduates shall have the ability to solve the complex engineering problems by applying electrical, mechanical, electronics and computer knowledge and engage in lifelong learning in their profession.

III. Graduates shall have the ability to lead and contribute in a team with entrepreneur skills, professional, social and ethical responsibilities.

IV. Graduates shall have ability to acquire scientific and engineering fundamentals necessary for higher studies and research.

PROGRAM OUTCOME (PO'S)

Engineering Graduates will be able to:

PO 1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOME(PSO'S)

PSO 1: Design and develop Mechatronics systems to solve the complex engineering problem by integrating electronics, mechanical and control systems.

PSO 2: Apply the engineering knowledge to conduct investigations of complex engineering problem related to instrumentation, control, automation, robotics and provide solutions.

COURSE OUTCOME

After the completion of the course the student will be able to

C204.1	Acquire the basic knowledge and application of diodes
C204.2	Understand the various biasing methods and hybrid model of BJT
C204.3	Acquire the knowledge about FET and various feedback topologies
C204.4	Recognize the working and characteristics of power amplifiers
C204.5	Explain the working and characteristics of various types of oscillators.
C204.6	Acquire the basic knowledge about UJT, timer IC555 and PLL.

CO VS PO'S AND PSO'S MAPPING

CO	PO1	PO 2	PO3	PO 4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PS0 1	PSO 2
C204. 1	3	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**1**
C204. 2	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**1**
C204. 3	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**1**
C204. 4	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**1**
C204. 5	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**2**
C204. 6	**3**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**2**	**2**

Note: H-Highly correlated=3, M-Medium correlated=2, L-Less correlated=1

SYLLABUS

Course code	Course Name	L-T-P - Credits	Year of Introduction
EC209	Analog Electronics	3-1-0-4	2016

Prerequisites :Nil

Course Objectives

- To familiarize basic electronic elements and their characteristics
- To develop understanding about BJT and FET circuits
- To understand the concept of power amplifier and differential amplifiers

Syllabus

Diode: Diode as a circuit element-diode clipping circuits-clamping circuits-voltage regulators-BJT: Operating point of a BJT-thermal runaway-h parameter model of a BJT-frequency response of amplifiers-FET: Construction and characteristics of JFET and MOSFET-Feedback: - Concepts – negative and positive feedback-Power Amplifiers- Class A, B, AB, C, D & S power amplifier-Differential Amplifiers:- The BJT differential pair- Large and small signal operation-MOS differential amplifier- Large and small signal operation-UJT- 555 Timer IC, PLL.

Expected outcome.

- Will get knowledge on electronic elements and their characteristics.

Text Book:

1. Allen Mottershead, *Electronic Devices and Circuits: An Introduction*, Prentice Hall of India.
2. V. Boylestad and Nashelsky, *Electronic Devices and Circuits*, Pearson Education
3. Ramakant A Gayakwad, *Op- Amps and Linear Integrated Circuits*, Prentice Hall of India

References:

1. Schilling and Belove, Electronic Circuits, McGraw Hill
2. Theodore F. Bogart Jr., Electronic Devices and Circuits,
3. Coughlin and Driscoll, Operational amplifiers and Linear Integrated Circuits,
4. K. R. Botkar, Integrated Circuits, Khanna Publishers
5. Somanathan Nair, Linear Integrated Circuits – Analsysis, Design & Application, Wiley-India

Course Plan

Module	Contents	Hours	Sem. Exam Marks
I	**Diode:** Diode as a circuit element - load line - piecewise linear model – single-phase half wave and full wave rectifier circuits – voltage regulation - ripple factor - rectifier efficiency - bridge rectifier - rectifier filters - diode clipping circuits - single level and two level clippers - clamping circuits –Zener diodes - Zener voltage regulators.	9	15%
II	**BJT:** Operating point of a BJT – DC biasing - bias stability - thermal runaway - AC Concepts –role of capacitors in amplifiers – common emitter AC equivalent circuit - amplifier gain and impedance calculations- h parameter model of a BJT –cascaded amplifiers, frequency response of amplifiers	9	15%

FIRST INTERNAL EXAMINATION			
III	**FET** Construction and characteristics of JFET and MOSFET, biasing a JFET and MOSFET, JFET and MOSFET small signal model - CS and CD amplifiers. feedback: - Concepts – negative and positive feedback feedback -feedback connection types - practical feedback circuits	9	15%
IV	**Power Amplifiers** Class A, B, AB, C, D & S power amplifiers - harmonic distortion efficiency -wide band amplifier - broad banding techniques - low frequency and high frequency compensation -cascode amplifier - broad banding using inductive loads - Darlington pairs.	10	15%
SECOND INTERNAL EXAMINATION			
V	**OSCILLATORS & MULTI VIBRATORS** Classification of oscillators – Barkhausen criteria- operation and analysis of RC phase shift – Hartely and Colpitts oscillators – Multi vibrators – astable, mono stable and bi stable multi vibrators	9	20%
VI	**UJT**-construction –working-UJT oscillator-UPS-brief overview of online UPS &off line UPS-SMPS-operation **Timer IC 555**: Functional diagram- astable and monostable modes **Phase Locked Loops**: Principles – building blocks of PLL-VCO-lock and capture ranges - capture process - frequency multiplication using PLL	10	20%
END SEMESTER EXAM			

QUESTION PAPER PATTERN

Maximum Marks : 100 Exam Duration:3 hours

PART A: FIVE MARK QUESTIONS
8 compulsory questions –1 question each from first four modules and 2 questions each from last two modules (8 x 5= 40 marks)

PART B: 10 MARK QUESTIONS
5 questions uniformly covering the first four modules. Each question can have maximum of three sub questions, if needed. Student has to answer any 3 questions
(3 x10 = 30 marks)

PART C: 15 MARK QUESTIONS
4 questions uniformly covering the last two modules. Each question can have maximum of four sub questions, if needed. Student has to answer any two questions
(2 x15 = 30 marks)

QUESTION BANK

MODULE I				
Q:NO:	**QUESTIONS**	**CO**	**KL**	
1	How can we use diode as a circuit element?	CO1	K2	
2	What is meant by load line concept in diode?	CO1	K1	
3	Write a short note on piece wise linear model of diode.	CO1	K2	
4	Describe working of half wave rectifier circuit.	CO1	K2	
5	Illustrate the working of centre tapped full wave rectifier circuit.	CO1	K2	
6	Illustrate the working of bridge rectifier circuit.	CO1	K5	
7	Derive an expression for ripple factor and efficiency of full wave rectifier.	CO1	K5	
8	Derive an expression for ripple factor and efficiency of half wave rectifier.	CO1	K5	
9	Explain various types of clippers and give a brief description about each clippers	CO1	K2	
10	Write a short note on clampers.	CO1	K1	
11	Give a brief description about zener diode.	CO1	K2	
12	Differentiate between zener breakdown and avalanche breakdown.	CO1	K2	

MODULE II				
1	Define and write a short note on operating point of BJT.	CO2	K2	
2	What are the different biasing methods, explain each.	CO2	K1	
3	Define Thermal runaway.	CO2	K1	
4	Briefly describe the role of capacitors in amplifier.	CO2	K2	
5	Illustrate the common emitter equivalent circuit.	CO2	K2	
6	Derive an eexpresssion for AC equivalent model of CE amplifier	CO2	K3	
7	Obtain the h parameter model of BJT	CO2	K2	
8	Explain about cascaded amplifier.	CO2	K2	
9	Briefly explain about frequency response of amplifier.	CO2	K2	
MODULE III				
1	Describe the construction and characteristics of JFET.	CO3	K2	
2	Describe the construction and characteristics of E-MOSFET.	CO3	K1	
3	Describe the construction and characteristics of D-MOSFET.	CO3	K5	
4	Explain various biasing methods of JFET.	CO3	K5	
5	Explain various biasing methods of MOSFET.	CO3	K5	
6	Briefly describe about common source amplifier.	CO3	K5	
7	Briefly describe about common drain	CO3	K4	

	amplifier.			
8	Differentiate negative and positive feedback concept.	CO3	K4	
9	Explain different types of negative feedback	CO3	K2	
MODULE IV				
1	Explain the operation and efficiency of Class A power amplifier with neat sketches.	CO4	K2	
2	With neat circuit diagram explain the working and efficiency of Class B amplifier	CO4	K6	
3	How can we eliminate the cross over distortion of Class B amplifier by using Class AB operation?	CO4	K2	
4	Construct a Class C amplifier and explain the working of the amplifier	CO4	K1	
5	Explain about harmonic distortion in amplifiers	CO4	K5	
6	How can we make a video amplifier using audio amplifier. Explain in detail	CO4	K2	
7	Explain the role of cascaded connection in amplifiers	CO4	K4	
8	Explain the working & operation of Darlington amplifier	CO4	K2	
9	With neat circuit diagram explain the working and efficiency of Class C amplifier	CO4	K2	
10	With neat circuit diagram explain the working and efficiency of Class D amplifier	CO4	K2	

MODULE V				
1	What are the classifications of oscillator?	CO5	K4	
2	Explain about the criteria for the oscillator circuits	CO5	K5	
3	Describe briefly about the working of RC Phase shift oscillator and how it satisfies the barkhausen criteria	CO5	K6	
4	Derive an expression to find out the frequency of RC phase shift oscillator	CO5	K2	
5	Explain with a neat circuit diagram about the Hartley oscillator and derive an expression for the frequency	CO5	K6	
6	Describe briefly about the Colpits oscillator and derive an expression for the frequency	CO5	K6	
7	Explain briefly about the working of astable multivibrator	CO5	K6	
8	Explain the working & operation of monostable multivibrator with a neat circuit diagram	CO5	K6	

MODULE VI				
1	Explain the construction and characteristics of UJT.	CO6	K5	
2	Give a brief description about UPS	CO6	K6	
3	Differentiate offline and online UPS.	CO3	K3	
4	Explain about SMPS with neat block diagram	CO6	K2	

5	Illustrate the functional diagram of IC555.	CO6	K6	
6	Describe how IC555 works as astable multivibrator.	CO6	K6	
7	Describe how IC555 works as monostable multivibrator.	CO6	K6	
8	Explain about PLL with neat block diagram.	CO6	K2	
9	Define capture range and lock range.	CO6	K2	
10	Write any one application of PLL.	CO6	K1	

APPENDIX 1

CONTENT BEYOND THE SYLLABUS

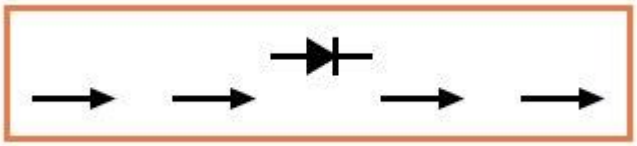
S:NO	TOPIC
1	WEIN BRIDGE OSCILLATOR
2	CRYSTAL OSCILLATOR
3	TUNNEL DIODE OSCILLATOR

Module 1

DIODE

Diode as a circuit element

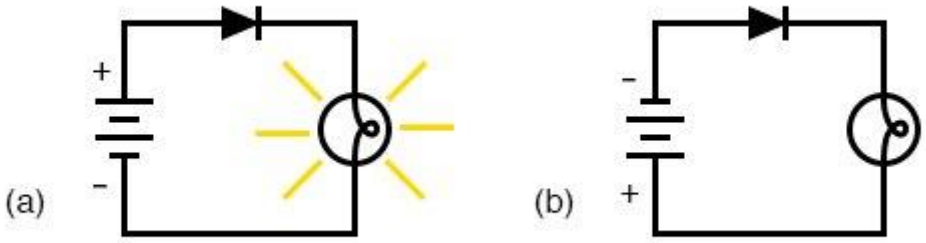
A diode is an electrical device allowing current to move through it in one direction with far greater ease than in the other. The most common kind of diode in modern circuit design is the semiconductor diode, although other diode technologies exist. Semiconductor diodes are symbolized in schematic diagrams such as the figure below. The term "diode" is customarily reserved for small signal devices, $I \leq 1$ A. The term rectifier is used for power devices, $I > 1$ A.



Semiconductor diode schematic symbol: Arrows indicate the direction of Current flow.

Semiconductor diode schematic symbol: Arrows indicate the direction of Current flow.

When placed in a simple battery-lamp circuit, the diode will either allow or prevent current through the lamp, depending on the polarity of the applied voltage. (figure below)



Diode operation: (a) Current flow is permitted; the diode is forward biased. (b) Current flow is prohibited; the diode is reversed biased.

When the polarity of the battery is such that current is allowed to flow through the diode, the diode is said to be forward-biased. Conversely, when the battery is "backward" and the diode blocks current, the diode is said to be reverse-biased. A diode may be thought of as like a switch: "closed" when forward-biased and "open" when reverse-biased.

The direction of the diode symbol's "arrowhead" points at the direction of the current in conventional flow. This convention holds true for all semiconductors possessing "arrowheads" in their schematics. The opposite is true when electron flow is used, where the current direction is against the "arrowhead".

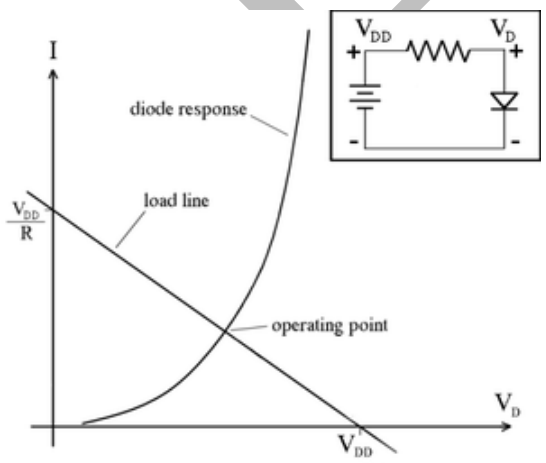
In graphical analysis of nonlinear electronic circuits, a load line is a line drawn on the characteristic curve, a graph of the current vs. the voltage in a nonlinear device like a diode or transistor. It represents the constraint put on the voltage and current in the nonlinear device by the external circuit. The load line, usually a straight line, represents the response of the linear part of the circuit, connected to the nonlinear device in question. The points where the characteristic curve and the load line intersect are the possible operating point(s) (Q points) of the circuit; at these points the current and voltage parameters of both parts of the circuit match.

The example at right shows how a load line is used to determine the current and voltage in a simple diode circuit. The diode, a nonlinear device, is in series with a linear circuit consisting of a resistor, R and a voltage source, VDD. The characteristic curve (curved line), representing the current I through the diode for any given voltage across the diode VD, is an exponential curve. The load line (diagonal line), representing the relationship between current and voltage due to Kirchhoff's voltage law applied to the resistor and voltage source, is

$$V_D = V_{DD} - IR$$

Since the current going through the three elements in series must be the same, and the voltage at the terminals of the diode must be the same, the operating point of the circuit will be at the intersection of the curve with the load line.

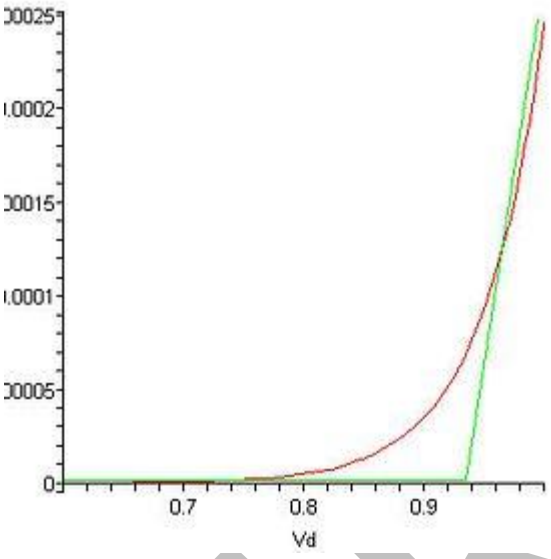
In a circuit with a three terminal device, such as a transistor, the current-voltage curve of the collector-emitter current depends on the base current. This is depicted on graphs by a series of (IC-VCE) curves at different base currents. A load line drawn on this graph shows how the base current will affect the operating point of the circuit.



Piecewise linear model

In practice, the graphical method is complicated and impractical for complex circuits. Another method of modeling a diode is called piecewise linear (PWL) modeling. In mathematics, this means taking a function and breaking it down into several linear segments. This method is used to approximate the diode characteristic curve as a series of linear segments. The real diode is modeled as 3 components in series: an ideal diode, a voltage source and a resistor.

The figure shows a real diode I-V curve being approximated by a two-segment piecewise linear model. Typically the sloped line segment would be chosen tangent to the diode curve at the Q-point. Then the slope of this line is given by the reciprocal of the small-signal resistance of the diode at the Q-point.



HALF WAVE RECTIFIER

A half wave rectifier is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half-cycle. Half-wave rectifiers are used to convert AC voltage to DC voltage, and only require a single diode to construct.

A rectifier is a device that converts alternating current (AC) to direct current (DC). It is done by using a diode or a group of diodes. Half wave rectifiers use one diode, while a full wave rectifier uses multiple diodes.

The working of a half wave rectifier takes advantage of the fact that diodes only allow current to flow in one direction.

Half Wave Rectifier Theory

A half wave rectifier is the simplest form of rectifier available. We will look at a complete half wave rectifier circuit later – but let's first understand exactly what this type of rectifier is doing.

The diagram below illustrates the basic principle of a half-wave rectifier. When a standard AC waveform is passed through a half-wave rectifier, only half of the AC waveform remains. Half-wave rectifiers only allow one half-cycle (positive or negative half-cycle) of the AC voltage through and will block the other half-cycle on the DC side, as seen below.

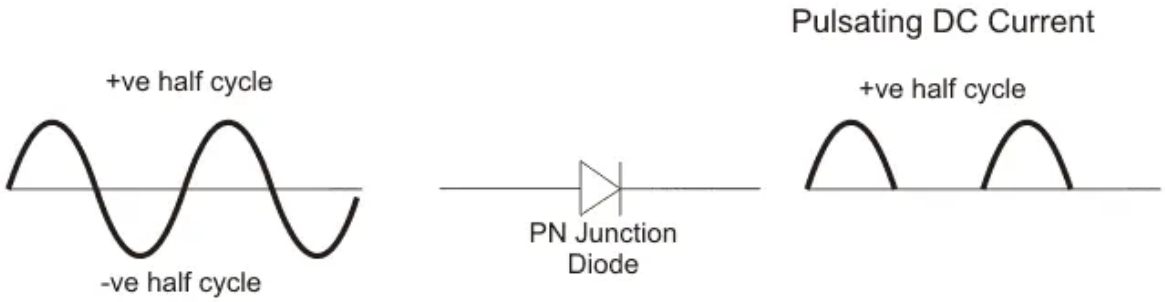


Figure - 1

Only one diode is required to construct a half-wave rectifier. In essence, this is all that the half-wave rectifier is doing.

Since DC systems are designed to have current flowing in a single direction (and constant voltage – which we'll describe later), putting an AC waveform with positive and negative cycles through a DC device can have destructive (and dangerous) consequences. So we use half-wave rectifiers to convert the AC input power into DC output power.

But the diode is only part of it – a complete half-wave rectifier circuit consists of 3 main parts:

1. A transformer
2. A resistive load
3. A diode

A half wave rectifier circuit diagram looks like this:

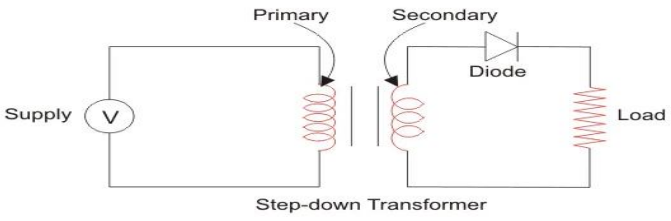


Figure - 2

First, a high AC voltage is applied to the to the primary side of the step-down transformer and we will get a low voltage at the secondary winding which will be applied to the diode.

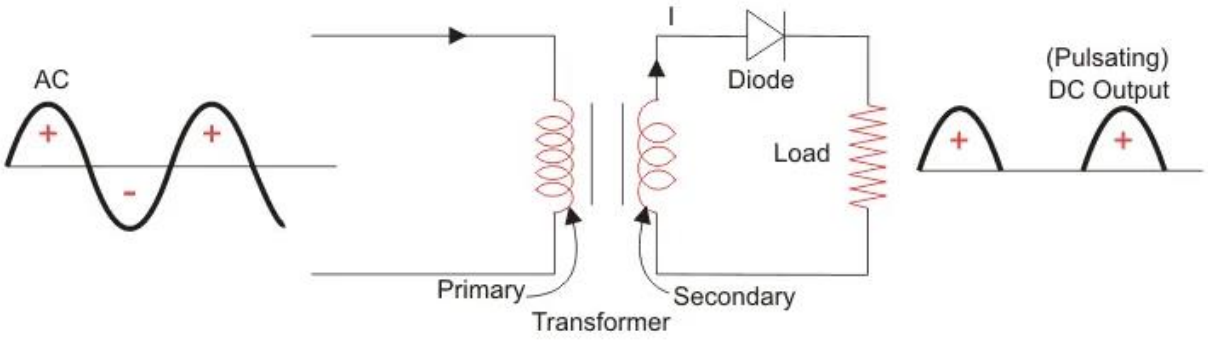


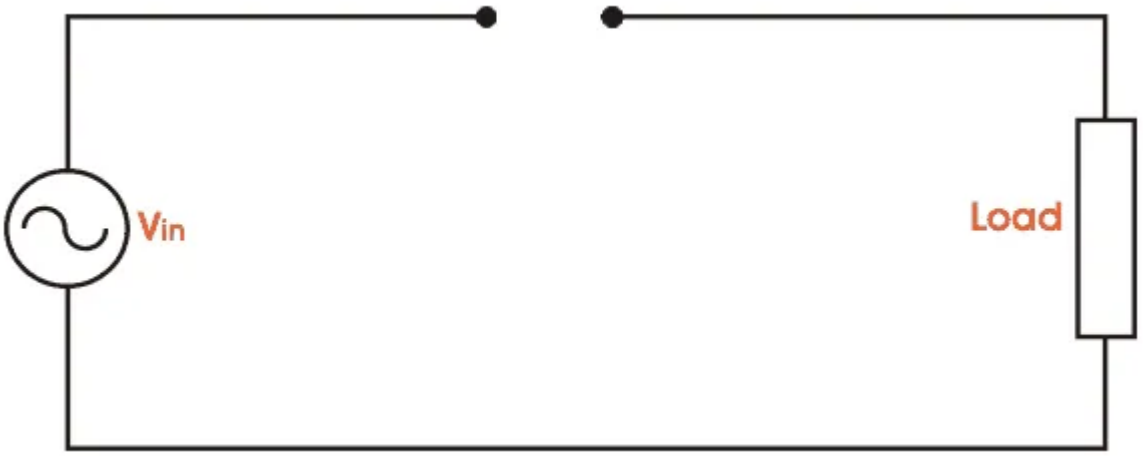
Figure - 3

During the positive half cycle of the AC voltage, the diode will be forward biased and the current flows through the diode. During the negative half cycle of the AC voltage, the diode will be reverse biased and the flow of current will be blocked. The final output voltage waveform on the secondary side (DC) is shown in figure 3 above.

For the positive half cycle of the AC source voltage, the equivalent circuit effectively becomes:

This is because the diode is forward biased, and is hence allowing current to pass through. So we have a closed circuit.

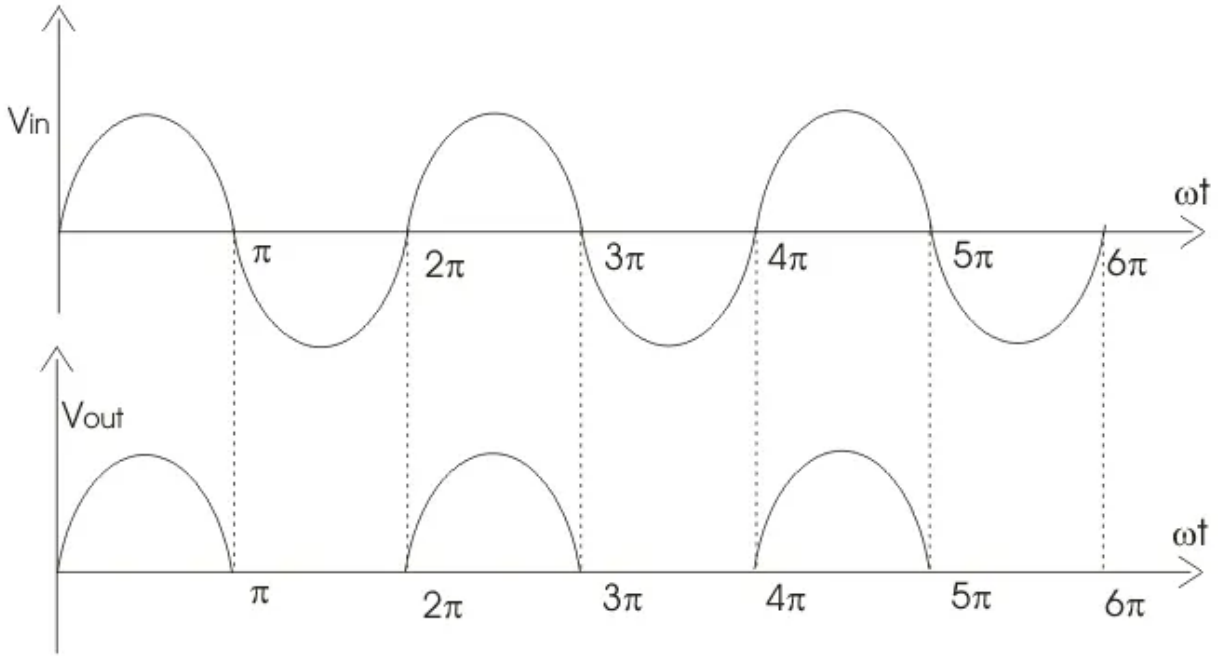
But for the negative half cycle of the AC source voltage, the equivalent circuit becomes:



Because the diode is now in reverse bias mode, no current is able to pass through it. As such, we now have an open circuit. Since current can not flow through to the load during this time, the output voltage is equal to zero.

This all happens very quickly – since an AC waveform will oscillate between positive and negative many times each second (depending on the frequency).

Here's what the half wave rectifier waveform looks like on the input side (Vin), and what it looks like on the output side (Vout) after rectification (i.e. conversion from AC to DC):



The graph above actually shows a positive half wave rectifier. This is a half-wave rectifier which only allows the positive half-cycles through the diode, and blocks the negative half-cycle.

To quantify how well the half-wave rectifier can convert the AC voltage into DC voltage, we use what is known as the ripple factor (represented by γ or r). The ripple factor is the ratio between the RMS value of the AC voltage (on the input side) and the DC voltage (on the output side) of the rectifier.

The formula for ripple factor is:

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

Which can also be rearranged to equal:

$$Ripple\ factor(r) = \frac{(I_{rms}^2 - I_{dc}^2)}{I_{dc}} = 1.21$$

The ripple factor of half wave rectifier is equal to 1.21 (i.e. $\gamma = 1.21$).

Note that for us to construct a good rectifier, we want to keep the ripple factor as low as possible. This is why we use capacitors and inductors as filters to reduce the ripples in the circuit.

Efficiency of Half Wave Rectifier

Rectifier efficiency (η) is the ratio between the output DC power and the input AC power. The formula for the efficieny is equal to:

$$\eta = \frac{P_{dc}}{P_{ac}}$$

The efficiency of a half wave rectifier is equal to 40.6% (i.e. $\eta_{max} = 40.6\%$)

RMS value of Half Wave Rectifier

To derive the RMS value of half wave rectifier, we need to calculate the current across the load. If the instantaneous load current is equal to $i_L = I_m \sin\omega t$, then the average of load current (I_{DC}) is equal to:

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t = \frac{I_m}{\pi}$$

Where I_m is equal to the peak instantaneous current across the load (I_{max}). Hence the output DC current (I_{DC}) obtained across the load is:

$$I_{DC} = \frac{I_{max}}{\pi},\ where\ I_{max} = maximum\ amplitude\ of\ dc\ current$$

For a half-wave rectifier, the RMS load current (Irms) is equal to the average current (IDC) multiple by π/2. Hence the RMS value of the load current (Irms) for a half wave rectifier is:

$$I_{rms} = \frac{I_m}{2}$$

Peak Inverse Voltage of Half Wave Rectifier

Peak Inverse Voltage (PIV) is the maximum voltage that the diode can withstand during reverse bias condition. If a voltage is applied more than the PIV, the diode will be destroyed.

Form Factor of Half Wave Rectifier

Form factor (F.F) is the ratio between RMS value and average value, as shown in the formula below:

$$F.F = \frac{RMS\ value}{Average\ value}$$

Output DC Voltage

The output voltage (VDC) across the load resistor is denoted by:

$$V_{DC} = \frac{V_{Smax}}{\pi},\ where\ V_{Smax} = maximum\ amplitude\ of\ secondary\ voltage$$

Applications of Half Wave Rectifier

Half wave rectifiers are not as commonly used as full-wave rectifiers. Despite this, they still have some uses:

For rectification applications

For signal demodulation applications

For signal peak applications

Advantages of Half Wave Rectifier

The main advantage of half-wave rectifiers is in their simplicity. As they don't require as many components, they are simpler and cheaper to setup and construct.

As such, the main advantages of half-wave rectifiers are:

Simple (lower number of components)

Cheaper up front cost (as their is less equipment. Although there is a higher cost over time due to increased power losses)

Disadvantages of Half Wave Rectifier

The disadvantages of half-wave rectifiers are:

They only allow a half-cycle through per sinewave, and the other half-cycle is wasted. This leads to power loss.

They produces a low output voltage.

The output current we obtain is not purely DC, and it still contains a lot of ripple (i.e. it has a high ripple factor)

The Full-wave Bridge Rectifier

Another type of circuit that produces the same output as a full-wave rectifier is that of the Bridge Rectifier (Fig. 1). This type of single phase rectifier uses 4 individual rectifying diodes connected in a "bridged" configuration to produce the desired output but does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown in figure. The 4 diodes labeled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in

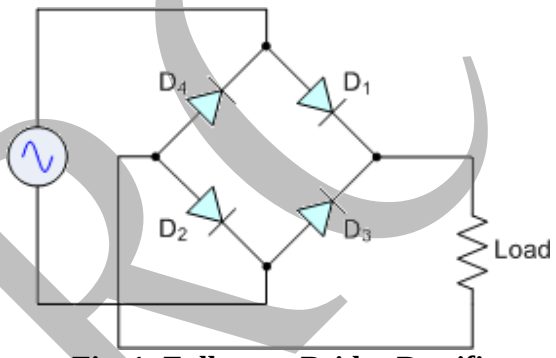


Fig. 1: Full-wave Bridge Rectifier

series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below (Fig. 2). During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch of as they are now reverse biased. The current flowing through the load is the same direction as before.

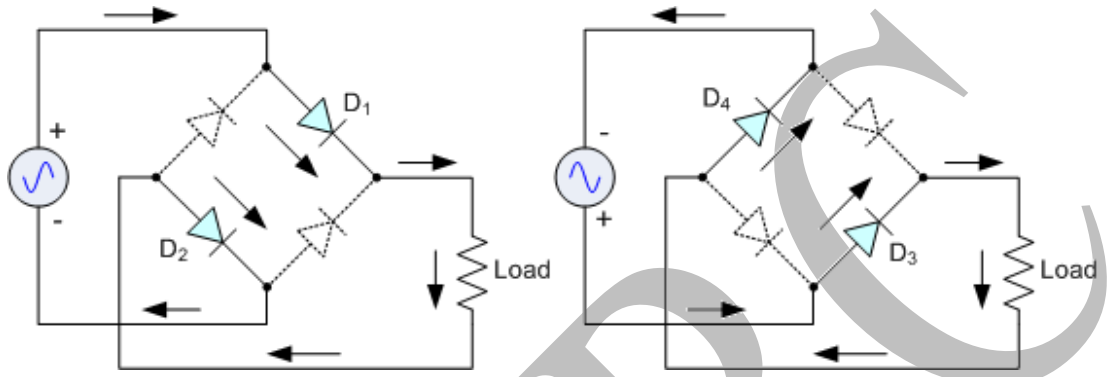


Fig. 2: Working of Full-wave bridge rectifier

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional during both the half cycles. Thus, the average dc output voltage across the load resistor is double that of a half-wave rectifier circuit, assuming no losses.

$$V_{dc} = \frac{2V_{max}}{\pi} = 0.637V_{max}$$

Ripple factor:

As mentioned in the previous lab the ripple factor is a measure of purity of the d.c. output of a rectifier and is defined as

$$r = \frac{V_{ac}(output)}{V_{dc}(output)} = \sqrt{\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2}} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1} = \sqrt{\left(\frac{0.707}{0.637}\right)^2 - 1} = 0.48$$

In case of a full-wave rectifier $V_{rms} = V_{max}/\sqrt{2} = 0.707V_{max}$. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply).

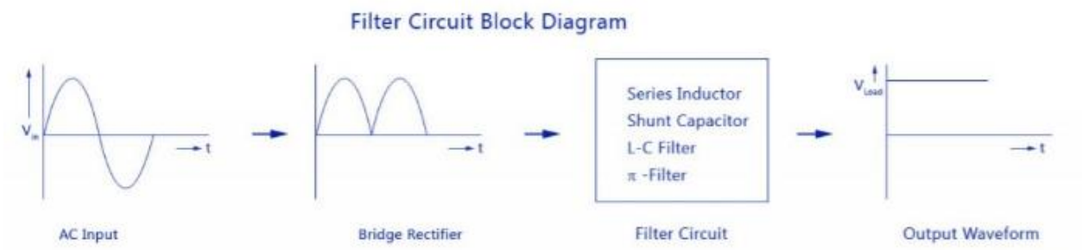
Rectification Efficiency:

Rectification efficiency, η, is given by

$$\eta = d.c.\,power\ delivered\ to\ load\,/\,a.c.\,power\ at\ input$$
$$= V_{dc} I_{dc} / V_{ac} I_{ac}$$
$$= \frac{V_{dc}^{\,2}/R_L}{V_s^{\,2}/(r_d + R_L)} = \frac{(0.637 V_{max})^2}{(0.707 V_{max})^2\left(1 + \frac{r_d}{R_L}\right)} = \frac{0.811}{\left(1 + \frac{r_d}{R_L}\right)}$$

where r_d is the forward resistance of diode. Under the assumption of no diode loss (r_d<<), the rectification efficiency in case of a full-wave rectifier is approximately 81.1%, which is twice the value for a half-wave rectifier.

RECTIFIER FILTERS



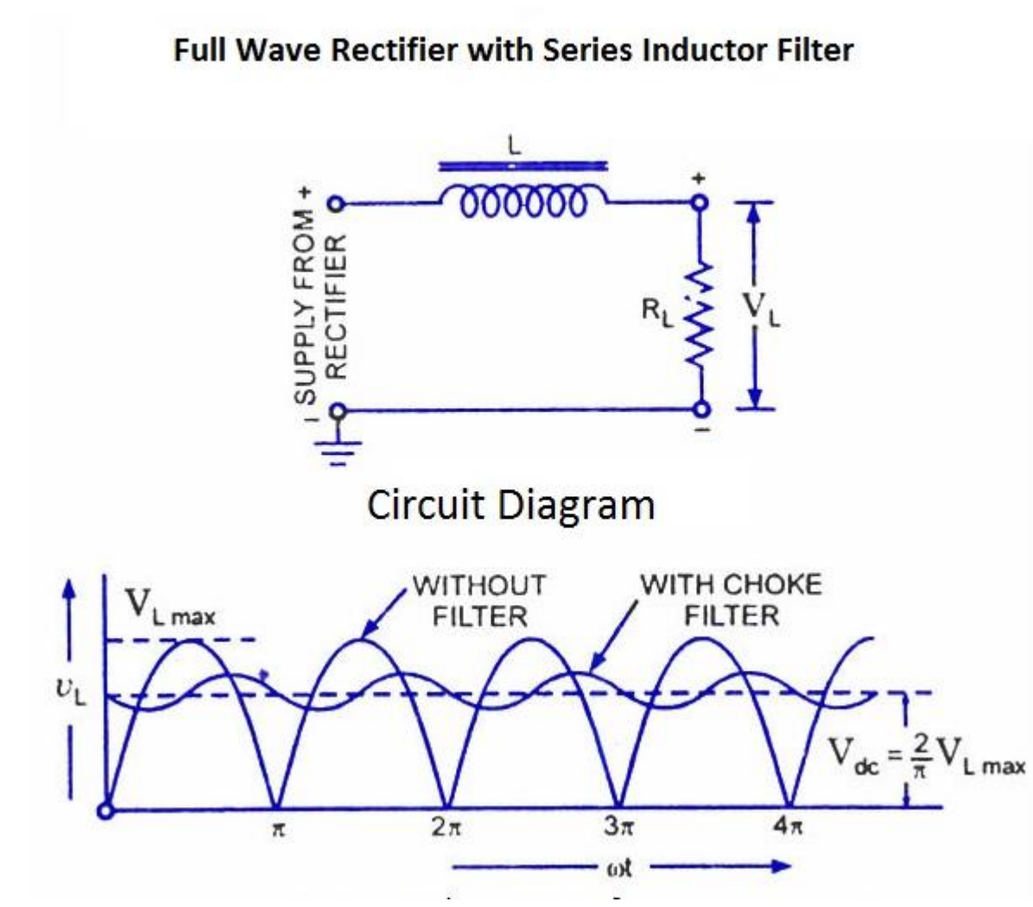
We have learnt in rectifier circuits about converting a sinusoidal ac voltage into its corresponding pulsating dc. Apart from the dc component, this pulsating dc voltage will have unwanted ac components like the components of its supply frequency along with its harmonics (together called ripples). These ripples will be the highest for a single-phase half wave rectifier and will reduce further for a single-phase full wave rectifier. The ripples will be minimum for 3-phase rectifier circuits. Such supply is not useful for driving complex electronic circuits. For most supply purposes constant dc voltage is required than the pulsating output of the rectifier. For most applications the supply from a rectifier will make the operation of the circuit poor. If the rectifier output is smoothened and steady and then passed on as the supply voltage, then the overall operation of the circuit becomes better. Thus, the output of the rectifier has to be passed though a filter circuit to filter the ac components.

The filter is a device that allows passing the dc component of the load and blocks the ac component of the rectifier output. Thus the output of the filter circuit will be a steady dc voltage.

The filter circuit can be constructed by the combination of components like capacitors, resistors, and inductors. Inductor is used for its property that it allows only dc components to pass and blocks ac signals. Capacitor is used so as to block the dc and allows ac to pass. All the combinations and their working are explained in detail below.

Series Inductor Filter

The circuit diagram of a full wave rectifier with a series inductor filter is given below.



As the name of the filter circuit suggests, the Inductor L is connected in series between the rectifier circuit and the load. The inductor carries the property of opposing the change in current that flows through it.

In other words, the inductor offers high impedance to the ripples and no impedance to the desired dc components. Thus the ripple components will be eliminated. When the rectifier output current increases above a certain value, energy is stored in it in the form of a magnetic field and this energy is given up when the output current falls below the average value. Thus all the sudden changes in current that occurs in the circuit will be smoothened by placing the inductor in series between the rectifier and the load.

The waveform below shows the use of inductor in the circuit.

From the circuit, for zero frequency dc voltage, the choke resistance Ri in series with the load resistance RL forms a voltage divider circuit, and thus the dc voltage across the load is

Vdc = RL/(Ri + RL)

Vdc is the output from a full wave rectifier. In this case, the value of Ri is negligibly small when compared to RL.

The effect of higher harmonic voltages can be easily neglected as better filtering for the higher harmonic components take place. This is because of the fact that with the increase in frequency, the reactance of the inductor also increases. It should be noted that a decrease in the value of load resistance or an increase in the value of load current will decrease the amount of ripples in the circuit. So, the series inductor filter is mostly used in cases of high load current or small load resistance. A simple series inductor filter may not be properly used. It is always better to use a shunt capacitor (C) with series inductor (L) to form an LC Filter.

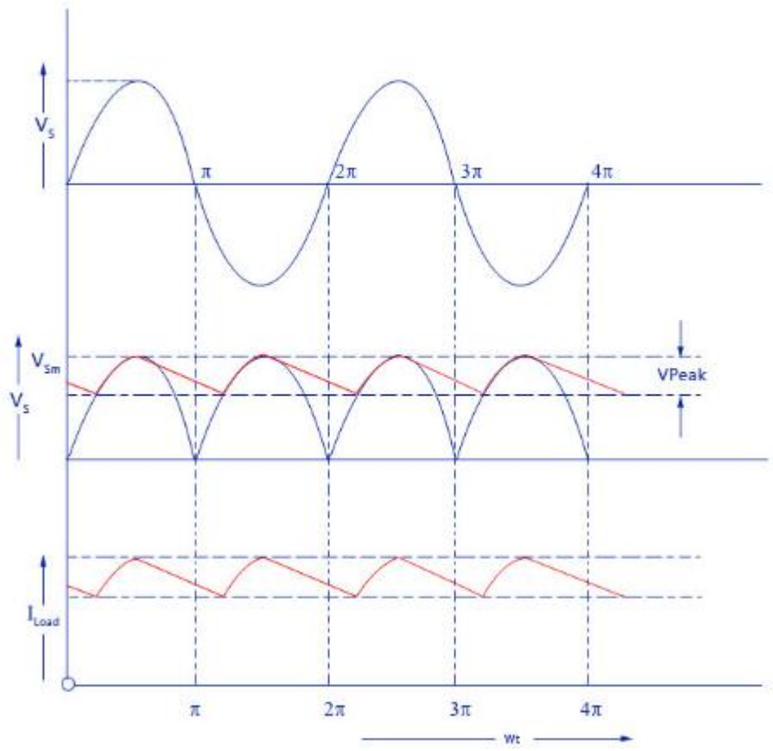
Shunt Capacitor Filter

As the name suggests, a capacitor is used as the filter and this high value capacitor is shunted or placed across the load impedance. This capacitor, when placed across a rectifier gets charged and stores the charged energy during the conduction period. When the rectifier is not conducting, this energy charged by the capacitor is delivered back to the load. Through this energy storage and delivery process, the time duration during which the current flows through the load resistor gets increased and the ripples are decreased by a great amount. Thus for the ripple component with a frequency of ‘f’ megahertz, the capacitor ‘C’ will offer a very low impedance. The value of this impedance can be written as:

Shunt Capacitor Impedance = 1/2 fC

Thus the dc components of the input signal along with the few residual ripple components, is only allowed to go through the load resistance RLoad. The high amount of ripple components of current gets bypassed through the capacitor C.

Fullwave Rectifier with Capacitor Filter - Waveform



The load current reduces by a smaller amount before the next pulse is received as there are 2 current pulses per cycle. This causes a good reduction in ripples and a further increase in the average dc load current.

L-C Filters

In the simple shunt capacitor filter circuit explained above, we have concluded that the capacitor will reduce the ripple voltage, but causes the diode current to increase .This large current may damage the diode and will further cause heating problem and decrease the efficiency of the filter. On the other hand, a simple series inductor reduces both the peak and effective values of the output current and output voltage. Then if we combine both the filter (L and C), a new filter called the L-C filter can be designed which will have a good efficiency, with restricted diode current and enough ripple removal factor .The voltage stabilizing action of shunt capacitor and the current smoothing action of series inductor filter can be combined to form a perfect practical filter circuit.

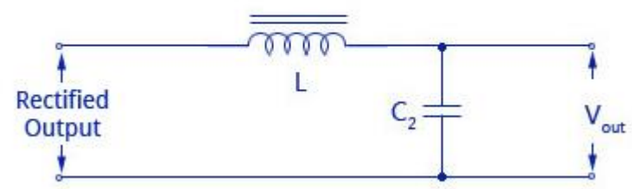
L-C filters can be of two types: Choke Input L-section Filter and L-C Capacitor input filter

Choke Input L-Section Filter

An inductor filter increases the ripple factor with the increase in load current Rload. A capacitor filter has an inversely proportional ripple factor with respect to load resistance. Economically, both inductor filter and capacitor filter are not suitable for high end purpose

L-C inductor input or L-section filter consists of an inductor ‘ L’ connected in series with a half or full wave rectifier and a capacitor ’C’ across the load. This arrangement is also called a choke input filter or L-section filter because it’s shape resembles and inverted L-shape. To increase the smoothing action using the filter circuit, just one L-C circuit will not be enough. Several L-section filters will be arranged to obtain a smooth filtered output. The circuit diagram and smoothened waveform of a Full wave rectifier output is shown below.

L-C Filter - Inductor input L Section Filter



As shown in the circuit diagram above, the inductor L allows the dc to pass but restricts the flow of ac components as its dc resistance is very small and ac impedance is large. After a signal passes through the choke, if there is any fluctuation remaining the current, it will be fully bypassed before it reaches the load by the shunt capacitor because the value of Xc is much smaller than Rload. The number of ripples can be reduced to a great amount by making the value of XL greater than Xc at ripple frequency.

Ripple Factor

Ripple Factor = Vac rms/Vdc = $(\sqrt{2}/3)(Xc/XL) = (\sqrt{2}/3)(1/[2wc])(1/[2wL]) = 1/(6\sqrt{2}w^2LC)$

Though the L-C filter has all these advantages, it has now become quite obsolete due the huge size of inductors and its cost of manufacturing. Nowadays, IC voltage regulators are more commonly used along with active filters, that reduce the ripples and keeps the output dc voltage constant.

The diagram of L-C Capacitor input filter and waveform is shown below.

Π – Filter or Capacitance Input Filter

The name pi – Filter implies to the resemblance of the circuit to a Π shape with two shunt capacitances (C1 and C2) and an inductance filter ‘L’. As the rectifier output is provided directly into the capacitor it also called a capacitor input filter.

When compared to other type of filters, the Π – Filter has some advantages like higher dc voltage and smaller ripple factor. But it also has some disadvantages like poor voltage regulation, high peak diode current, and high peak inverse voltage.

This filter is divided into two – a capacitor filter and a L-section filter. The capacitor C1 does most of the filtering in the circuit and the remaining ripple os removed by the L-section filter (L-C2). C1 is selected to provide very low reactance to the ripple frequency. The voltage regulation is poor for this circuit as the output voltage falls off rapidly with the increase in load current.

Ripple Factor

Ripple Factor = $\sqrt{2}/(8w^3C1C2LRload)$

DIODE CLIPPING CIRCUITS

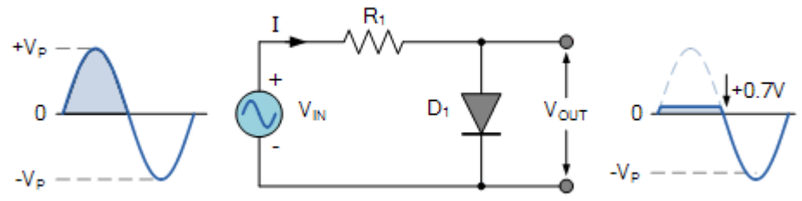
This clipping of the input signal produces an output waveform that resembles a flattened version of the input. For example, the half-wave rectifier is a clipper circuit, since all voltages below zero are eliminated.

But **Diode Clipping Circuits** can be used a variety of applications to modify an input waveform using signal and Schottky diodes or to provide over-voltage protection using zener diodes to ensure that the output voltage never exceeds a certain level protecting the circuit from high voltage spikes. Then diode clipping circuits can be used in voltage limiting applications.

We saw in the *Signal Diodes* tutorial that when a diode is forward biased it allows current to pass through itself clamping the voltage. When the diode is reverse biased, no current flows through it and the voltage across its terminals is unaffected, and this is the basic operation of the diode clipping circuit.

Although the input voltage to diode clipping circuits can have any waveform shape, we will assume here that the input voltage is sinusoidal. Consider the circuits below.

Positive Diode Clipping Circuits

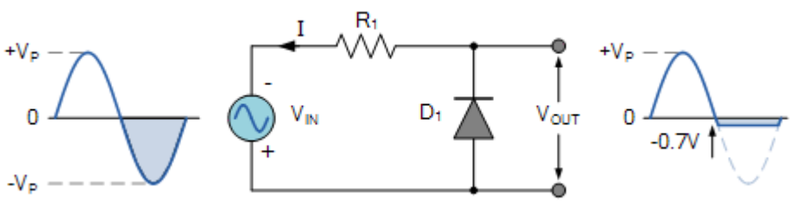


In this diode clipping circuit, the diode is forward biased (anode more positive than cathode) during the positive half cycle of the sinusoidal input waveform. For the diode to become forward biased, it must have the input voltage magnitude greater than +0.7 volts (0.3 volts for a germanium diode).

When this happens the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value. Thus the output voltage which is taken across the diode can never exceed 0.7 volts during the positive half cycle.

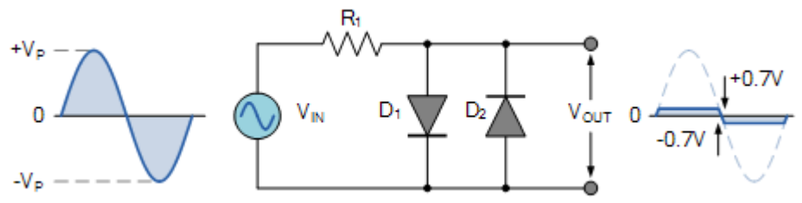
During the negative half cycle, the diode is reverse biased (cathode more positive than anode) blocking current flow through itself and as a result has no effect on the negative half of the sinusoidal voltage which passes to the load unaltered. Thus the diode limits the positive half of the input waveform and is known as a positive clipper circuit.

Negative Diode Clipping Circuits



Here the reverse is true. The diode is forward biased during the negative half cycle of the sinusoidal waveform and limits or clips it to –0.7 volts while allowing the positive half cycle to pass unaltered when reverse biased. As the diode limits the negative half cycle of the input voltage it is therefore called a negative clipper circuit.

Clipping of Both Half Cycles



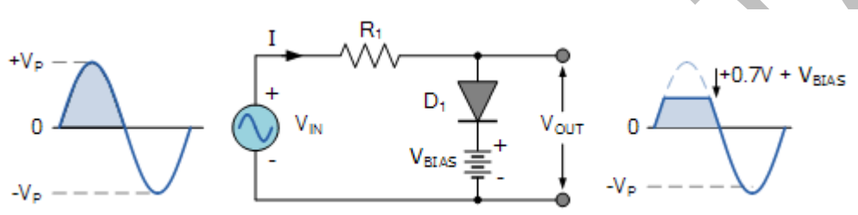
If we connected two diodes in inverse parallel as shown, then both the positive and negative half cycles would be clipped as diode D_1 clips the positive half cycle of the sinusoidal input waveform while diode D_2 clips the negative half cycle. Then diode clipping circuits can be used to clip the positive half cycle, the negative half cycle or both.

For ideal diodes the output waveform above would be zero. However, due to the forward bias voltage drop across the diodes the actual clipping point occurs at +0.7 volts and –0.7 volts respectively. But we can increase this ±0.7V threshold to any value we want up to the maximum value, (V_{PEAK}) of the sinusoidal waveform either by connecting together more diodes in series creating multiples of 0.7 volts, or by adding a voltage bias to the diodes.

Biased Diode Clipping Circuits

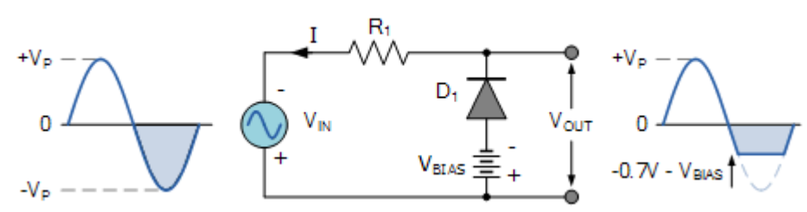
To produce diode clipping circuits for voltage waveforms at different levels, a bias voltage, V_{BIAS} is added in series with the diode to produce a combination clipper as shown. The voltage across the series combination must be greater than V_{BIAS} + 0.7V before the diode becomes sufficiently forward biased to conduct. For example, if the V_{BIAS} level is set at 4.0 volts, then the sinusoidal voltage at the diode's anode terminal must be greater than **4.0 + 0.7 = 4.7 volts** for it to become forward biased. Any anode voltage levels above this bias point are clipped off.

Positive Bias Diode Clipping



Likewise, by reversing the diode and the battery bias voltage, when a diode conducts the negative half cycle of the output waveform is held to a level $-V_{BIAS} - 0.7V$ as shown.

Negative Bias Diode Clipping



A variable diode clipping or diode limiting level can be achieved by varying the bias voltage of the diodes. If both the positive and the negative half cycles are to be clipped, then two biased clipping diodes are used. But for both positive and negative diode clipping, the bias voltage need not be the same.

CLAMPER CIRCUIT

A Clamper Circuit is a circuit that adds a DC level to an AC signal. Actually, the positive and negative peaks of the signals can be placed at desired levels using the clamping circuits. As the DC level gets shifted, a clamper circuit is called as a **Level Shifter**.

Clamper circuits consist of energy storage elements like capacitors. A simple clamper circuit comprises of a capacitor, a diode, a resistor and a dc battery if required.

A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.

In order to maintain the time period of the wave form, the **tau** must be greater than, half the time period dischargingtimeofthecapacitorshouldbeslow.dischargingtimeofthecapacitorshouldbeslow.

$$\tau=RC$$

Where

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used

The time constant of charge and discharge of the capacitor determines the output of a clamper circuit.

- In a clamper circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.

- The load resistor and the capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.

The DC component present in the input is rejected when a capacitor coupled network is used as a capacitor blocks dc as a capacitor blocks dc. Hence when **dc** needs to be **restored**, clamping circuit is used.

Types of Clampers

There are few types of clamper circuits, such as

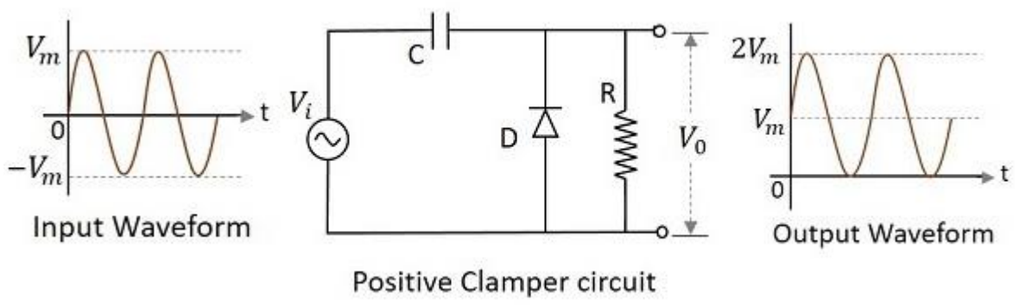
- Positive Clamper
- Positive clamper with positive Vr
- Positive clamper with negative Vr
- Negative Clamper
- Negative clamper with positive Vr
- Negative clamper with negative Vr

Let us go through them in detail.

Positive Clamper Circuit

A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be **positively clamped**.

A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal. The figure below explains the construction of a positive clamper circuit.



Positive Clamper circuit

Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time. During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The capacitor is now charged to its peak value Vm. The diode is forward biased and conducts heavily.

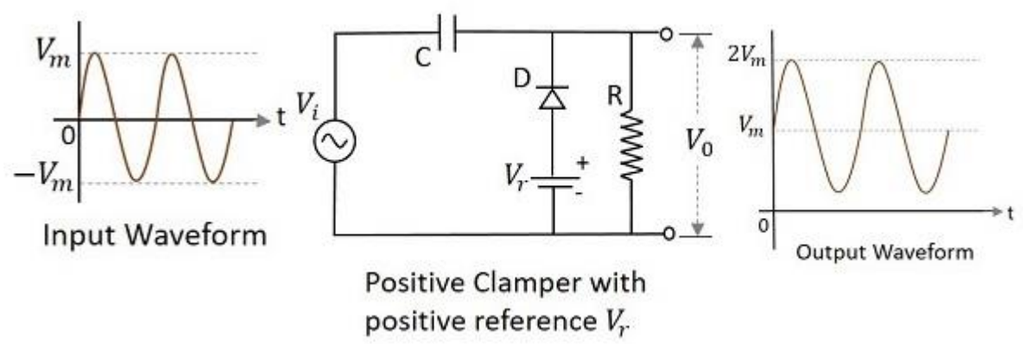
During the next positive half cycle, the capacitor is charged to positive Vm while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

V0=Vi+VmV0=Vi+Vm

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Positive Clamper with Positive V_r

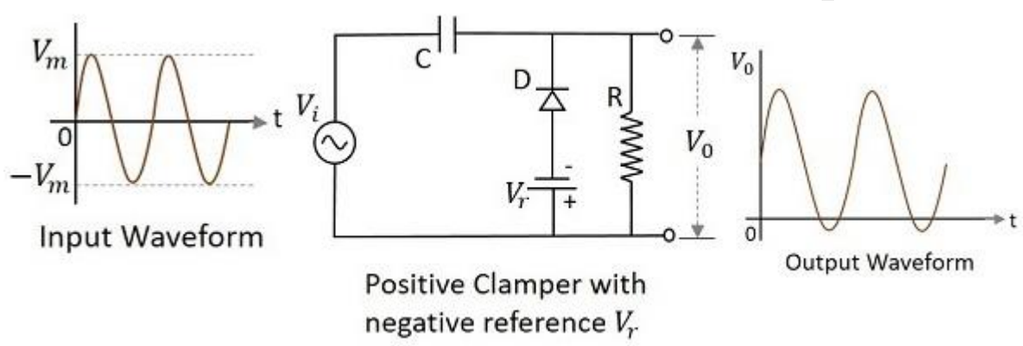
A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.



Positive Clamper with positive reference V_r

Positive Clamper with Negative Vr

A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

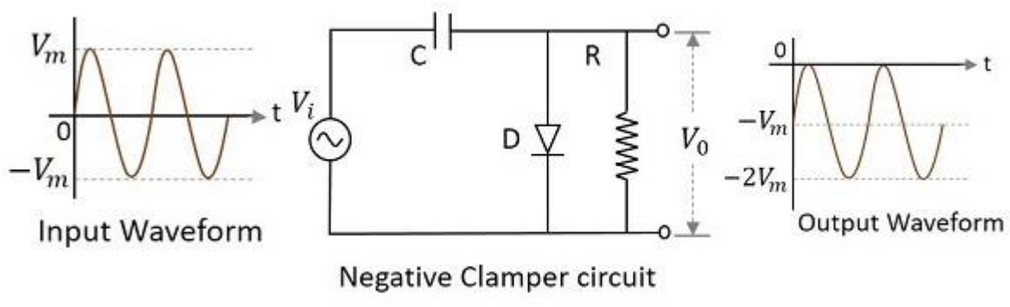


Positive Clamper with negative reference V_r

During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level. During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage. These changes make the output voltage as shown in the above figure.

Negative Clamper

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. The figure below explains the construction of a negative clamper circuit.



Negative Clamper circuit

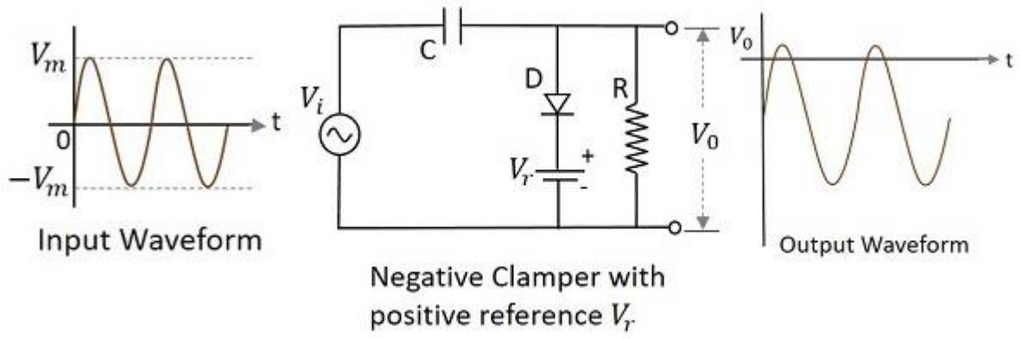
During the positive half cycle, the capacitor gets charged to its peak value Vm. The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

V0=Vi+VmV0=Vi+Vm

Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Negative clamper with positive V_r

A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with positive reference voltage is constructed as below.



Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive. During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied. During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

ZENER DIODE

A Zener diode is a special type of diode designed to reliably allow current to flow "backwards" when a certain set reverse voltage, known as the *Zener voltage*, is reached.

Zener diodes are manufactured with a great variety of Zener voltages and some are even variable. Some Zener diodes have a sharp, highly doped p–n junction with a low Zener voltage, in which case the reverse conduction occurs due to electron quantum tunnelling in the short space between p and n regions − this is known as the Zener effect, after Clarence Zener. Diodes with a higher Zener voltage have a more gradual junction and their mode of operation also involves avalanche breakdown. Both breakdown types are present in Zener diodes with the Zener effect predominating at lower voltages and avalanche breakdown at higher voltages.

Zener diodes are widely used in electronic equipment of all kinds and are one of the basic building blocks of electronic circuits. They are used to generate low-power stabilized supply rails from a higher voltage and to provide reference voltages for circuits, especially stabilized power supplies. They are also used to protect circuits from overvoltage, especially electrostatic discharge (ESD).

A conventional solid-state diode allows significant current if it is reverse-biased above its reverse breakdown voltage. When the reverse bias breakdown voltage is exceeded, a conventional diode is subject to high current due to avalanche breakdown. Unless this current is limited by circuitry, the diode may be permanently damaged due to overheating. A Zener diode exhibits almost the same properties, except the device is specially designed so as to have a reduced breakdown voltage, the so-called Zener voltage. By contrast with the conventional device, a reverse-biased Zener diode exhibits a controlled breakdown and allows the current to keep the voltage across the Zener diode close to the Zener breakdown voltage. For example, a diode with a Zener breakdown voltage of 3.2 V exhibits a voltage drop of very nearly 3.2 V across a wide range of reverse currents. The Zener diode is therefore ideal for applications such as the generation of a reference voltage (e.g. for an amplifier stage), or as a voltage stabilizer for low-current applications.

Another mechanism that produces a similar effect is the avalanche effect as in the avalanche diode. The two types of diode are in fact constructed the same way and both effects are present in diodes of this type. In silicon diodes up to about 5.6 volts, the Zener effect is the predominant effect and shows a marked negative temperature coefficient. Above 5.6 volts, the avalanche effect becomes predominant and exhibits a positive temperature coefficient.

In a 5.6 V diode, the two effects occur together, and their temperature coefficients nearly cancel each other out, thus the 5.6 V diode is useful in temperature-critical applications. An alternative, which is used for voltage references that need to be highly stable over long periods of time, is to use a Zener diode with a temperature coefficient (TC) of +2 mV/°C (breakdown voltage 6.2–6.3 V) connected in series with a forward-biased silicon diode (or a transistor B-E junction) manufactured on the same chip. The forward-biased diode has a temperature coefficient of −2 mV/°C, causing the TCs to cancel out. The circuit symbol shows below:

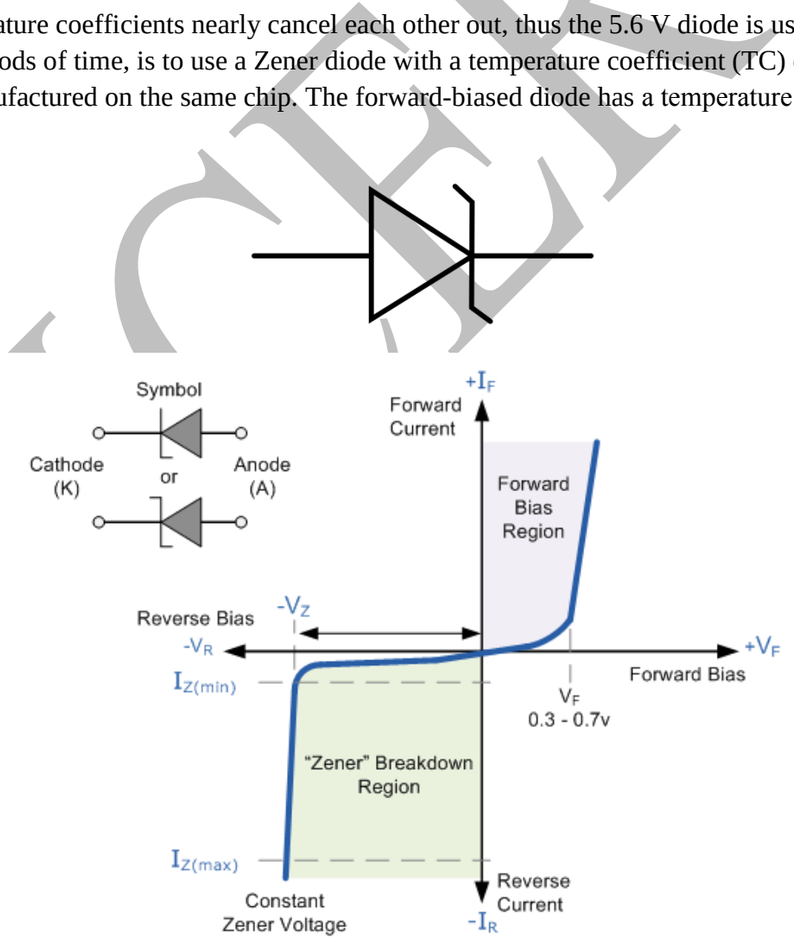
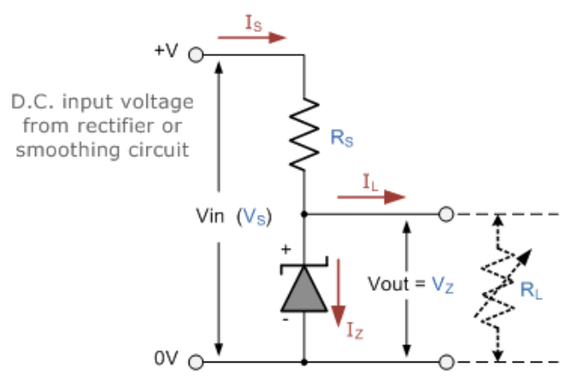


Fig: Characteristic of a Zener diode

The Zener Diode Regulator

Zener Diodes can be used to produce a stabilised voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor (R_S), the zener diode will conduct sufficient current to maintain a voltage drop of Vout.

We remember from the previous tutorials that the DC output voltage from the half or full-wave rectifiers contains ripple superimposed onto the DC voltage and that as the load value changes so to does the average output voltage. By connecting a simple zener stabiliser circuit as shown below across the output of the rectifier, a more stable output voltage can be produced.



Resistor, R_S is connected in series with the zener diode to limit the current flow through the diode with the voltage source, V_S being connected across the combination. The stabilised output voltage V_{out} is taken from across the zener diode.

The zener diode is connected with its cathode terminal connected to the positive rail of the DC supply so it is reverse biased and will be operating in its breakdown condition. Resistor R_S is selected so to limit the maximum current flowing in the circuit.

With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the zener diode which in turn dissipates its maximum power. Also a small value of the series resistor R_S will result in a greater diode current when the load resistance R_L is connected and large as this will increase the power dissipation requirement of the diode so care must be taken when selecting the appropriate value of series resistance so that the zener's maximum power rating is not exceeded under this no-load or high-impedance condition.

The load is connected in parallel with the zener diode, so the voltage across R_L is always the same as the zener voltage, ($V_R = V_Z$). There is a minimum zener current for which the stabilisation of the voltage is effective and the zener current must stay above this value operating under load within its breakdown region at all times. The upper limit of current is of course dependant upon the power rating of the device. The supply voltage V_S must be greater than V_Z.

One small problem with zener diode stabiliser circuits is that the diode can sometimes generate electrical noise on top of the DC supply as it tries to stabilise the voltage. Normally this is not a problem for most applications but the addition of a large value decoupling capacitor across the zener's output may be required to give additional smoothing.

Then to summarise a little. A zener diode is always operated in its reverse biased condition. As such a simple voltage regulator circuit can be designed using a zener diode to maintain a constant DC output voltage across the load in spite of variations in the input voltage or changes in the load current.

The zener voltage regulator consists of a current limiting resistor R_S connected in series with the input voltage V_S with the zener diode connected in parallel with the load R_L in this reverse biased condition. The stabilised output voltage is always selected to be the same as the breakdown voltage V_Z of the diode.

MODULE 2

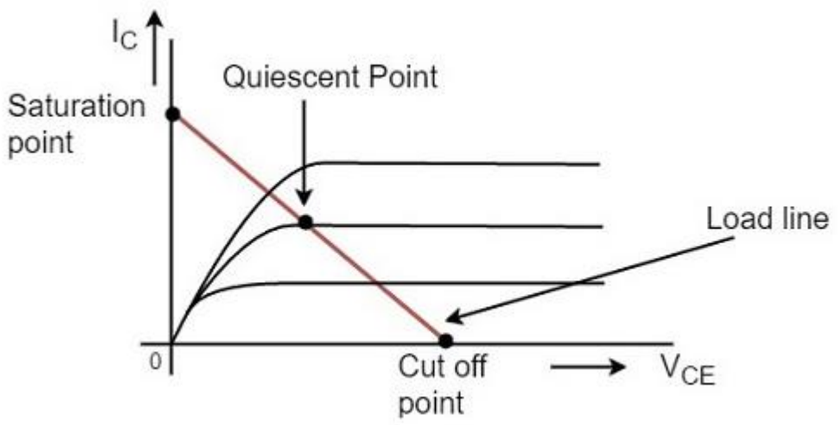
BJT

Operating Point of BJT

When a line is drawn joining the saturation and cut off points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.

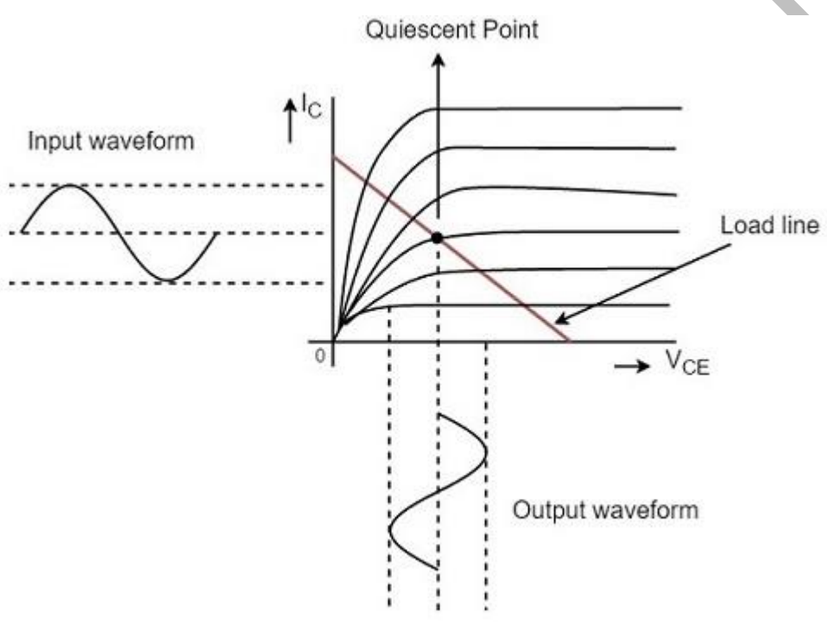
The following graph shows how to represent the operating point.



Faithful Amplification

The process of increasing the signal strength is called as **Amplification**. This amplification when done without any loss in the components of the signal, is called as **Faithful amplification**.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.



In the above graph, the input signal applied is completely amplified and reproduced without any losses. This can be understood as **Faithful Amplification**.

The operating point is so chosen such that it lies in the **active region** and it helps in the reproduction of complete signal without any loss.

DC Biasing

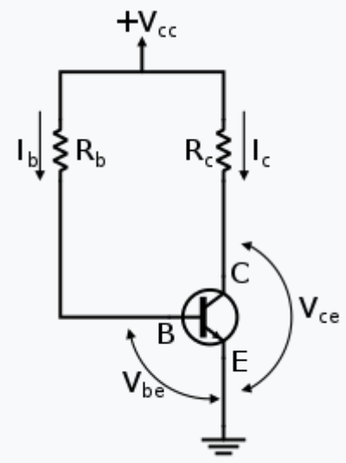
The bias circuit stabilizes the operating point of the transistor for variations in transistor characteristics and operating temperature. The gain of a transistor can vary significantly between different batches, which results in widely different operating points for sequential units in serial production or after replacement of a transistor. Due to the Early effect, the current gain is affected by the collector–emitter voltage. Both gain and base–emitter voltage depend on the temperature. The leakage current also increases with temperature. A bias network is selected to reduce effects of device variability, temperature, and voltage changes.[1]

A bias circuit may be composed of only resistors, or may include elements such as temperature-dependent resistors, diodes, or additional voltage sources, depending on the range of operating conditions expected

The following discussion treats five common biasing circuits used with class-A bipolar transistor amplifiers:

1. Fixed bias
2. Collector-to-base bias
3. Fixed bias with emitter resistor
4. Voltage divider bias or potential divider
5. Emitter bias

Fixed bias (base bias)



Fixed bias (Base bias)

This form of biasing is also called *base bias or fixed resistance biasing*. In the example image on the right, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$$V_{cc} = I_b R_b + V_{be}$$

Therefore,

$$I_b = (V_{cc} - V_{be})/R_b$$

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_b, the base current I_b is fixed. Therefore, this type is called *fixed bias* type of circuit.

Also, for the given circuit,

$$V_{cc} = I_c R_c + V_{ce}$$

Therefore,

$$V_{ce} = V_{cc} - I_c R_c$$

The common-emitter current gain of a transistor is an important parameter in circuit design, and is specified on the data sheet for a particular transistor. It is denoted as β on this page.

Because

$$I_c = \beta I_b$$

we can obtain I_c as well. In this manner, operating point given as (V_{ce},I_c) can be set for given transistor.

Advantages:

- The operating point is set by a single resistor R_B and the calculation is very simple.

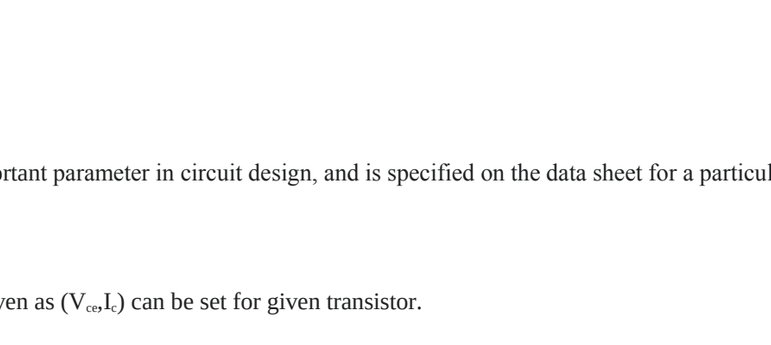
Disadvantages:

- Since the bias is set by the base current, the collector current is directly proportional to β. Therefore, the operating point will vary significantly when transistors are swapped and it is unstable under changes in temperature.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Usage:

Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where the transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

Collector feedback bias



Collector-to-base bias

This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor is connected to the collector instead of connecting it to the DC source . So any thermal runaway will induce a voltage drop across the resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b} across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Advantages:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor).
- Circuit stabilizes the operating point against variations in Vcc.

Disadvantages:

- Although small changes in β are OK, large changes in β will greatly change the operating point. Rb must be chosen once β is known fairly accurately (perhaps within ~ 25%), yet the variability of β between "identical" parts is often larger than this.

- In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_e} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

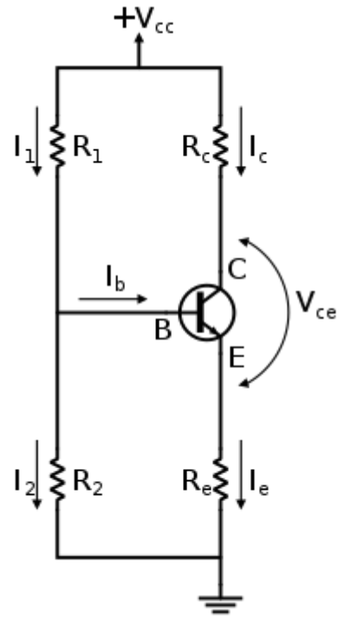
$$\beta R_e \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_e fairly large or making R_b very low.
  - If R_e is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
  - If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.

- The resistor Rb causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability. However, a T (R-C-R) network can be used to reduce the AC feedback, which however poses a heavier load on the collector than the simple feedback resistor. At higher frequencies a R-L feedback network can be used, however, it will introduce peaking into the frequency response at various points.

Usage: The negative feedback also increases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

Voltage divider biasing or emitter bias



Voltage divider bias

The voltage divider is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current, provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor. The voltage divider configuration achieves the correct voltages by the use of resistors in certain patterns. By manipulating the resistors in certain ways you can achieve more stable current levels without having β value affect it too much.

In this circuit the base voltage is given by:

$$V_B = \text{ voltage across } R_2 = V_{cc}\frac{R_2}{(R_1 + R_2)} - I_b\frac{R_1 R_2}{(R_1 + R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1 + R_2)} \text{ provided } I_b << I_1 = V_b/R_1 \ .$$

Also $V_B = V_{be} + I_e R_e$

For the given circuit,

$$I_b = \frac{\frac{V_{cc}}{1+R_1/R_2} - V_{be}}{(\beta + 1)R_e + R_1 \parallel R_2}.$$

Advantages:

- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Disadvantages:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_c = \beta I_b = \beta\frac{\frac{V_{cc}}{1+R_1/R_2} - V_{be}}{(\beta + 1)R_e + R_1 \parallel R_2} \approx \frac{\frac{V_{cc}}{1+R_1/R_2} - V_{be}}{R_e},$$

which is approximately the case if

$$(\beta + 1)R_e >> R_1 \parallel R_2$$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \parallel R_2$ very low.
  - If R_E is of large value, high V_{cc} is necessary. This increases cost as well as precautions necessary while handling.
  - If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises Vb closer to V_c, reducing the available swing in collector voltage, and limiting how large Rc can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.
- AC as well as DC feedback is caused by R_e, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage:

The circuit's stability and merits as above make it widely used for linear circuits.

Thermal Runaway

At constant current, the voltage across the emitter–base junction V_{BE} of a bipolar transistor *decreases* by 2 mV (silicon) and 1.8 mV (germanium) for each 1 °C rise in temperature (reference being 25 °C). By the Ebers–Moll model, if the base–emitter voltage V_{BE} is held constant and the temperature rises, the current through the base–emitter diode I_B will increase, and thus the collector current I_C will also increase. Depending on the bias point, the power dissipated in the transistor may also increase, which will further increase its temperature and exacerbate the problem. This deleterious positive feedback results in **thermal runaway**. There are several approaches to mitigate bipolar transistor thermal runaway. For example,

- Negative feedback can be built into the biasing circuit so that increased collector current leads to decreased base current. Hence, the increasing collector current throttles its source.
- Heat sinks can be used that carry away extra heat and prevent the base–emitter temperature from rising.
- The transistor can be biased so that its collector is normally less than half of the power supply voltage, which implies that collector–emitter power dissipation is at its maximum value. Runaway is then impossible because increasing collector current leads to a decrease in dissipated power; this notion is known as the *half-voltage principle.*

The circuits below primarily demonstrate the use of negative feedback to prevent thermal runaway.

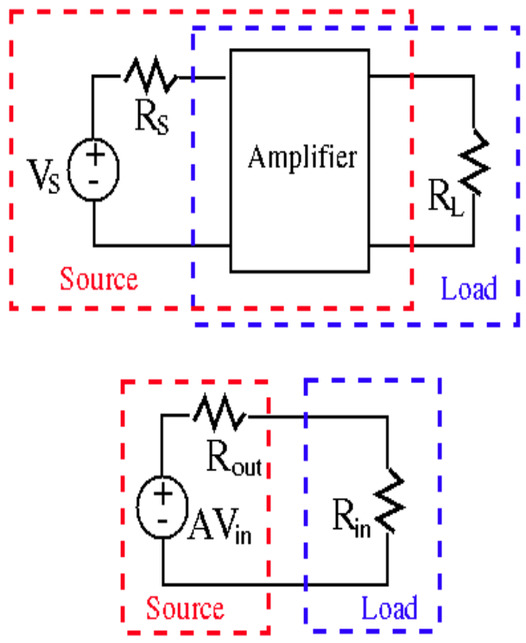
Role of capacitors in amplifier

Capacitors are fundamental components in both analog and digital electronic circuits. These passive components play an important role in influencing the operational behavior of circuits. The characteristics of a capacitor vary mainly depending on the dielectric material used. The dielectric material determines the capacitance value, energy efficiency, and size of a capacitor. Fixed value capacitors can be broadly categorized into two: polar and non-polar capacitors. Non-polar capacitors include ceramic, film, and paper capacitors. Aluminium electrolytic capacitors and tantalum capacitors are polar components.

In circuits, capacitors are used for a wide range of applications including storing electrical charges, blocking DC components, bypassing AC components, filtering unwanted signals, and so on. The applications of a capacitor primarily depend on its characteristics. Key properties to consider when selecting a capacitor for a given application include capacitance value, voltage rating, frequency response characteristics, cost, and physical size. Other properties of a capacitor that can influence the performance of an electronic circuit include temperature characteristics, self-healing properties, aging, and flammability.

AC equivalent circuits

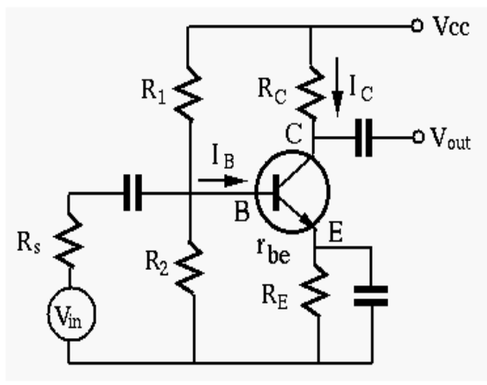
The transistor amplifier in the example here has a voltage gain of 150, based on the assumption of zero internal resistance $R_S = 0$ in its source and infinite load resistance $R_L = \infty$. But, as discussed before, the voltage a circuit receives from a source depends on its input impedance r_{in} as well as the internal impedance $R_s \neq 0$ of the source, while the voltage it delivers depends on its output impedance r_{out} as well as the load impedance R_L. It is therefore important to consider these input and output impedances of an amplification circuit as well as its voltage gain.



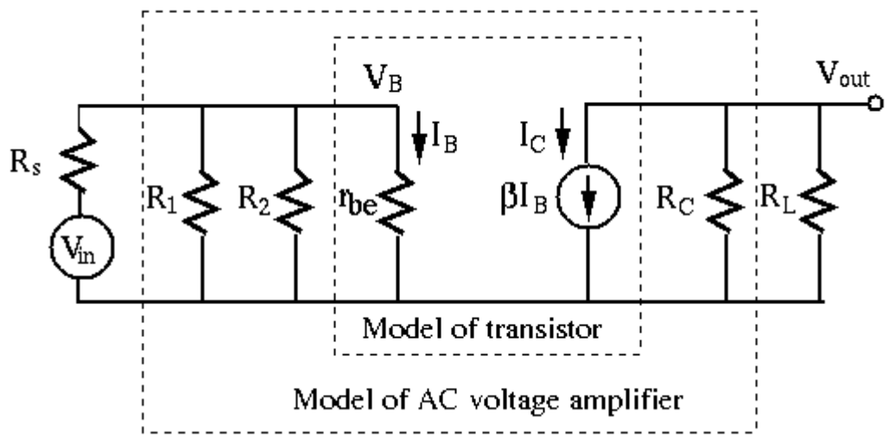
In the first figure, everything inside the red box, including the amplifier as well as V_S and R_s, is treated as the source, while everything inside the blue box, including the amplifier as well as R_L, is treated as the load. Given the amplifier as well as the source V_S and R_s, and the load R_L, we need to find the following three parameters so that the red and blue boxes in the first figure can be modeled by the corresponding boxes in the second figure:

- Input impedance r_{in}
- Output impedance r_{out}
- voltage gain A

Consider the typical transistor AC amplification circuit below:



If the capacitances of the coupling capacitors and the emitter by-pass capacitor are large enough with respect to the frequency of the AC signal in the circuit is high enough, these capacitors can all be approximated as short circuit. Moreover, note that the AC voltage of the voltage supply V_{CC} is zero, it can be treated the same as the ground. Now the AC behavior of the transistor amplification circuit can be modeled by the following small signal equivalent circuit:



Amplifier gain and Impedance Calculation

- **AC Input Impedance:**

  For AC signals, the input of the amplification circuit is shown below, where R_s is the internal resistance of the signal source, and the input impedance of the circuit is the three resistances R_1, R_2 and r_{be} in parallel:

$$r_{in} = R_1||R_2||r_{be} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{r_{be}}\right)^{-1} = \frac{R_1 R_2 r_{be}}{R_1 R_2 + R_1 r_{be} + R_2 r_{be}} \approx r_{be} \tag{68}$$

  The approximation is due to the fact that typically $R_1,\ R_2 \gg r_{be}$.

- **AC Output Impedance:**

  This is simply the resistance of the resistor $r_{out} = R_C$.

- **AC Voltage Gain:**

  Given the AC input voltage v_{in}, the base voltage and current are

$$v_b \approx v_{in}\,\frac{r_{be}}{r_{be} + R_s}, \qquad i_b = \frac{v_b}{r_{be}} \approx \frac{v_{in}}{r_{be} + R_s} \tag{69}$$

  The collector current is $i_c = \beta i_b$ and collect voltage is

$$v_{out} = v_c \approx -i_c\,(R_C||R_L) = -\beta\, i_b\,(R_C||R_L) = -\beta\frac{v_{in}}{r_{be} + R_s}(R_C||R_L) \tag{70}$$

Here the negative sign indicates the fact that v_c is $180°$ out of phase with v_b. The voltage gain is:

$$A = \frac{v_{out}}{v_{in}} = \frac{v_c}{v_{in}} \approx -\beta\frac{R_C||R_L}{r_{be} + R_s} \tag{71}$$

If

$$R_s \ll r_{in} = R_1||R_2||r_{be} \approx r_{be}, \qquad R_L \gg r_{out} = R_C \tag{72}$$

then the gain can be approximated as

$$A = \frac{v_{out}}{v_{in}} \approx -\beta \frac{R_C}{r_{be}} \tag{73}$$

To achieve higher gain A, we want to have smaller r_{be} and greater R_C. However, this also means the input resistance $r_{in} \approx r_{be}$ is small and the output resistance $r_{out} \approx R_C$ is large, neither is desirable.

Note that r_{be} is not constant. As shown before, $r_{be} \approx \eta \, V_T / I_B$ of the base-emitter PN-junction is approximately inversely proportional to I_B.

Also note that R_C and I_B affects the DC operating point. Distortion may be caused if R_C or I_B is set properly.

Hybrid Parameters

Hybrid parameters (also known as h parameters) are known as 'hybrid' parameters as they use Z parameters, Y parameters, voltage ratio, and current ratios to represent the relationship between voltage and current in a two port network. H parameters are useful in describing the input-output characteristics of circuits where it is hard to measure Z or Y parameters (such as in a transistor).

H parameters encapsulate all the important linear characteristics of the circuit, so they are very useful for simulation purposes. The relationship between voltages and current in h parameters can be represented as:

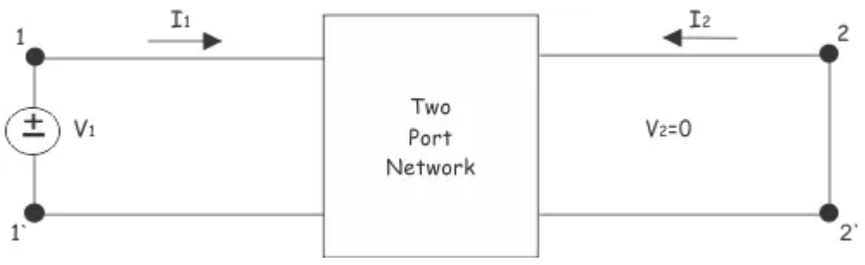
$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

This can be represented in matrix form as:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

How to Find H Parameters in Two Port Networks

Let us short circuit the output port of a two port network as shown below,



Now, ratio of input voltage to input current, at short circuited output port is:

$$\left.\frac{V_1}{I_1}\right|_{V_2 = 0} = h_{11}$$

This is referred to as the short circuit input impedance. Now, the ratio of the output current to input current at the short-circuited output port is:

$$\left.\frac{I_2}{I_1}\right|_{V_2 = 0} = h_{21}$$

This is called short-circuit current gain of the network. Now, let us open circuit the port 1. At that condition, there will be no input current (I_1=0) but open circuit voltage V_1 appears across the port 1, as shown below:

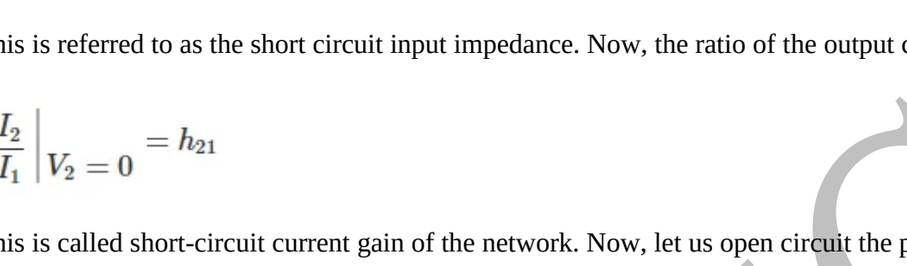
$$\left.\frac{V_1}{V_2}\right|_{I_1 = 0} = h_{12} = \textit{open circuit reverse voltage gain}$$

This is referred as reverse voltage gain because, this is the ratio of input voltage to the output voltage of the network, but voltage gain is defined as the ratio of output voltage to the input voltage of a network.

$$\left.\frac{I_2}{V_2}\right|_{I_1 = 0} = h_{21}$$

It is referred as open circuit output admittance

$$V_1 = h_{11} I_1 + h_{12} V_2 \cdots\cdots\cdots\cdots\cdots (i)$$
$$I_2 = h_{21} I_1 + h_{22} V_2 \cdots\cdots\cdots\cdots\cdots (ii)$$



The h parameters equivalent network of a two port network

Cascaded amplifier

The cascade of a Common Emitter amplifier stage followed by a Common Collector (emitter-follower) amplifier stage can provide a good overall voltage amplifier, figure 10.1.1. The Common Emitter input resistance is relatively high and Common Collector output resistance is relatively low. The voltage follower second stage, Q_2, contributes no increase in voltage gain but provides a near voltage-source (low resistance) output so that the gain is nearly independent of load resistance. The high input resistance of the Common Emitter stage, Q_1, makes the input voltage nearly independent of input-source resistance. Multiple Common Emitter stages can be cascaded with emitter follower stages inserted between them to reduce the attenuation due to inter-stage loading.

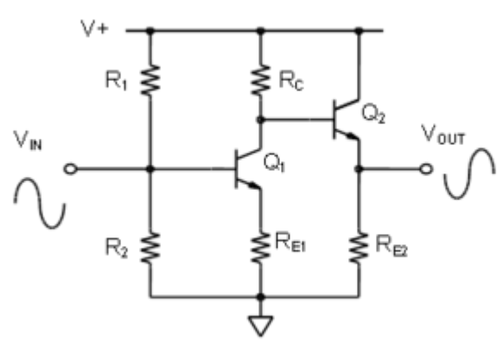


Figure 10.1.1 Common Emitter, Common Collector

Frequency response of Amplifier

Emitter bypass capacitors are used to short circuit the emitter resistor and thus increases the gain at high frequency. The coupling and bypass capacitors cause the fall of the signal in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitances are effectively open circuits.

In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence the mid band frequency gain is maximum.

At the high frequencies, the bypass and coupling capacitors are replaced by short circuits. The stray capacitors and the transistor determine the response.

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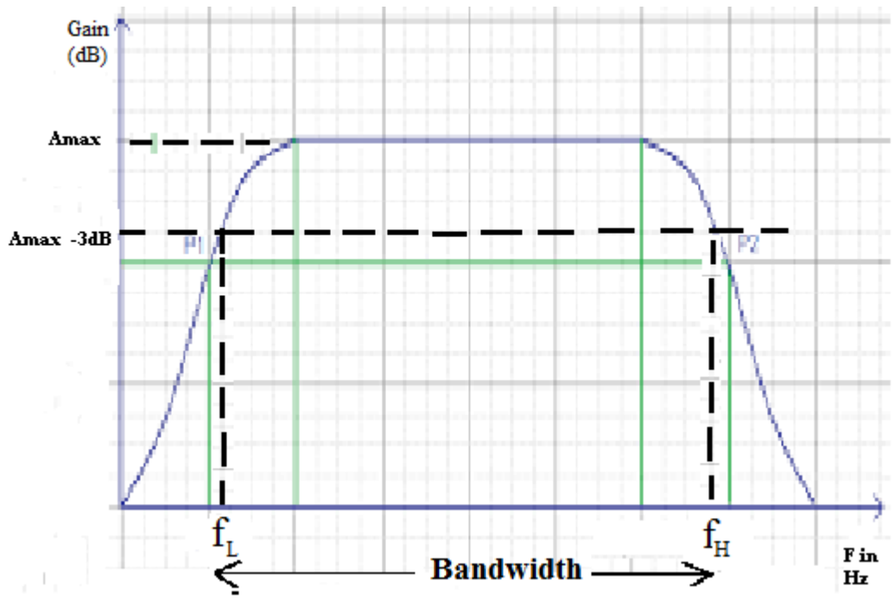


Calculations from the graph

Bandwidth = $f_H - f_L$ (in Hz)

MODULE 3

FET

Junction Field Effect Transistor (JFET)

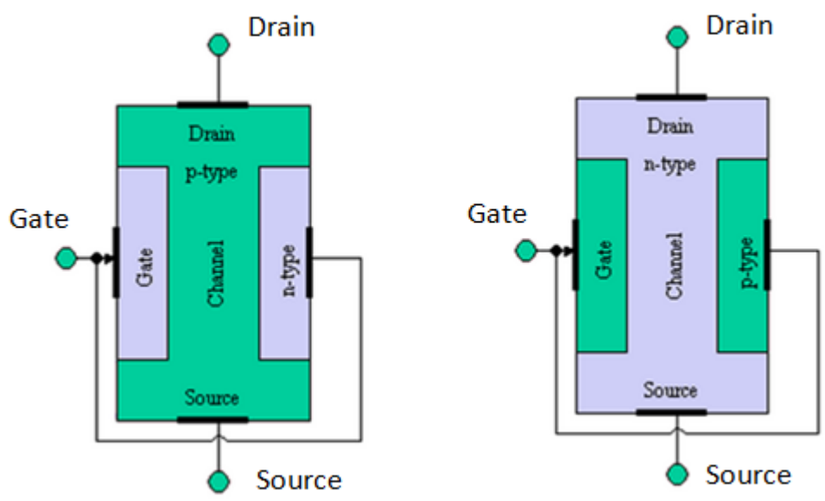
A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes.

The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device.

The JFET has high input impedance and low noise level.

Construction Details:

A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in fig.1.



The bar forms the conducting channel for the charge carriers.

If the bar is of p-type, it is called p-channel JFET as shown in fig.1(i) and if the bar is of n-type, it is called n-channel JFET as shown in fig.1(ii).

The two pn junctions forming diodes are connected internally and a common terminal called gate is taken out.

Other terminals are source and drain taken out from the bar as shown in fig.1.

Thus a JFET has three terminals such as , gate (G), source (S) and drain (D).

JFET Polarities

Fig.2 (i) shows the n-channel JFET polarities and fig.2 (ii) shows the p-channel JFET polarities.

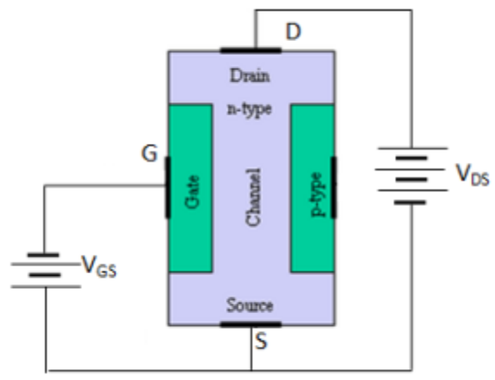


Fig.2 (i)

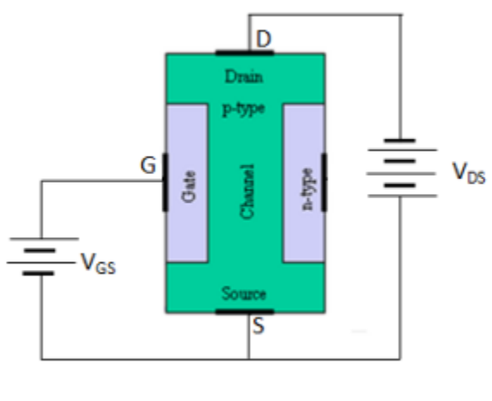


Fig.2 (ii)

In each case, the voltage between the gate and source is such that the gate is reverse biased.

The source and the drain terminals are interchangeable.

The following points may be noted:

1. The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance.
2. The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.
3. In all JFETs, source current I_S is equal to the drain current i.e $I_S = I_D$.

Principle and Working of JFET

Principle of JEFT

Fig.3 shows the circuit of n-channel JFET with normal polarities.

The two pn junctions at the sides form two depletion layers.

The current conduction by charge carriers (i.e. electrons) is through the channel between the two depletion layers and out of the drain.

The width and hence resistance of this channel can be controlled by changing the input voltage V_{GS}.

The greater the reverse voltage V_{GS}, the wider will be the depletion layer and narrower will be the conducting channel.

The narrower channel means greater resistance and hence source to drain current decreases.

Reverse will happen when V_{GS} decreases.

Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.

In other word, the magnitude of drain current I_D can be changed by altering V_{GS}.

Working of JEFT

The working of JFET can be explained as follows:

Case-i:

When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero as shown in fig.3(i), the two pn junctions at the sides of the bar establish depletion layers.

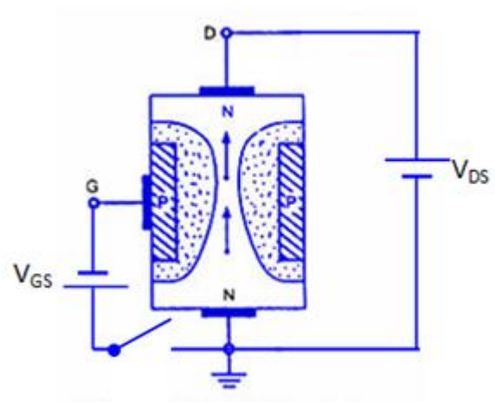


Fig.3 (i)

The electrons will flow from source to drain through a channel between the depletion layers.

The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

Case-ii:

When a reverse voltage V_{GS} is applied between gate and source terminals, as shown in fig.3(ii), the width of depletion layer is increased.

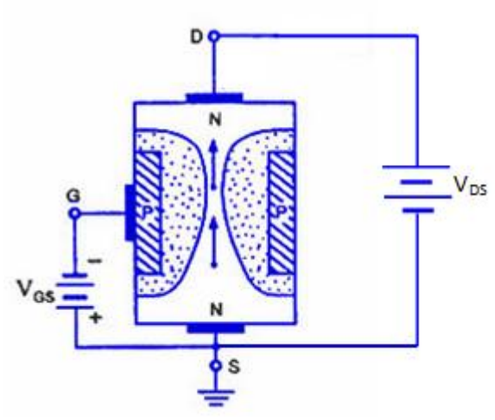


Fig.3 (ii)

This reduces the width of conducting channel, thereby increasing the resistance of n-type bar.

Consequently, the current from source to drain is decreased.

On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases.

This increases the width of the conducting channel and hence source to drain current.

A p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and polarities of V_{GS} and V_{DS} are reversed.

Schematic Symbol of JFET

Fig.4 shows the schematic symbol of JFET.

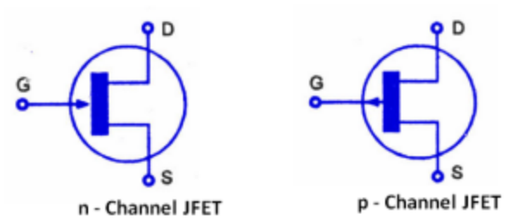


Fig.4

Difference Between JFET and BJT

The JFET differs from an ordinary BJT in the following ways:

1. In a JFET, there is only one type of carrier,i.e. holes in p-type channel and electrons in n-type channel. For this reason it is also called unipolar transistor.However, in an ordinary BJT, both electrons and holes play role in conduction. Therefore, it is called as bipolar transistor.
2. As the input circuit of a JFET is reverse biased, therefore, it has a high input impedance. However, the input circuit of a BJT is forward biased and hence has low input impedance.
3. The primary functional difference between the JFET and BJT is that no current enters the gate of JFET. However, in typical BJT base current might be a few μA.
4. A BJT uses the current into its base to control a large current between collector and emitter. Whereas a JFET uses voltage on the gate terminal to control the current between drain and source.
5. In JFET, there is no junction. Therefore, noise level in JFET is very small.

Advantages of JFET

A JFET is a voltage controlled, constant current device in which variation in input voltage control the output current. Some of the advantages of JFET are:

1. It has a very high input impedance. This permits high degree of isolation between the input and output circuits.
2. The operation of a JFET depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes and those of transistors are not present in a JFET.
3. A JFET has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.
4. A JFET has a very high power gain. This eliminates the necessity of using driver stages.
5. A JFET has a smaller size, longer life and high efficiency

Output Characteristics of JFET

The curve between drain current, I_D and drain-source voltage, V_{DS} of a JFET at constant gate-source voltage, V_{GS} is known as output characteristics of JFET.

Drain Characteristic With Shorted-Gate

Fig.1shows the drain characteristic with shorted-gate.

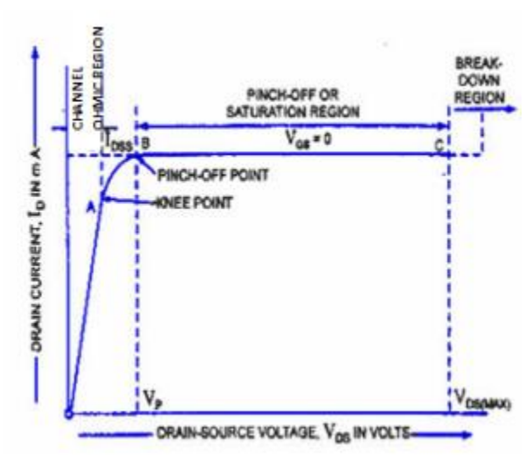


Fig.1 (ii)

when drain-source voltage V_{DS} is zero, there is no attracting potential at the drain, so no current flows inspite of the fact that the channel is fully open. So, drain current $I_D = 0$.

For small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the drain current increases linearly with the increase in V_{DS}, upto the knee point.

This region, to the left of the knee point of the curve is called the channel ohmic *region, as* in this region the JFET behaves like an ordinary resistor.

With the increase in drain current I_D, the ohmic voltage drop between the source and channel region reverse-biases the gate junction.

The reverse-biasing of the gate junction is not uniform throughout. The reverse bias is more at the drain end than at the source end of the channel.

So with the increase in V_{DS}, the conducting portion of the channel begins to constrict more at the drain end. Eventually a voltage V_{DS} is reached at which the channel is pinched off.

The drain current I_D no longer increases with the increase in V_{DS}. It approaches a constant saturation value.

The value of voltage V_{DS} at which the channel is pinched off i.e. all the free charges from the channel get removed, and the drain current I_D attains a constant value, is called the *pinch-off voltage* V_p.

From point A (knee point) to the point B (pinch-off point) the drain current I_D increases with the increase In voltage V_{DS} following a reverse square law.

The region of the characteristic in which drain current I_D remains fairly constant is called *the pinch-off region.* It is also sometimes called the *saturation region* or *amplifier region.*

In this region the JFET operates as a *constant current device since* drain current (or output current) remains almost constant. It is the normal operating region of the JFET where it is used as an amplifier.

The drain current in the pinch-off region with $V_{GS} = 0$ is referred to the *drain-source saturation current, I_{DSS}*).

Drain current in the pinch-of region is given by Shockley's equation:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

Where I_D = Drain current at given V_{GS}

I_{DSS} = Shorted – gate drain current

V_{GS} = gate-source Voltage

$V_{GS(off)}$ = gate-source cut off voltage

If drain-source voltage, V_{DS} is continuously increased, a stage comes when the gate-channel junction breaks down. At this point current increases very rapidly. and the JFET may be destroyed. This happens because the charge carriers making up the saturation current at the gate channel junction accelerate to a high velocity and produce an *avalanche effect.*

Drain Characteristics With External Bias

The circuit diagram for determining the drain characteristics with different values of external bias is shown in Fig.2(i). and a family of drain characteristics for different values of gate-source voltage V_{GS} is shown in Fig.2(ii).

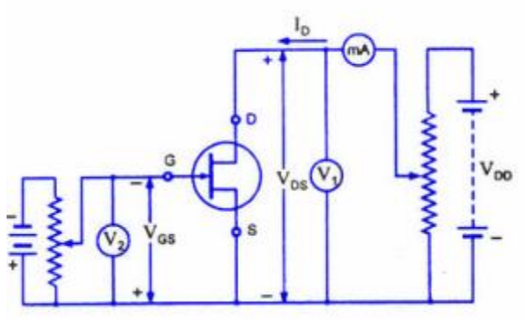


Fig.2 (i)

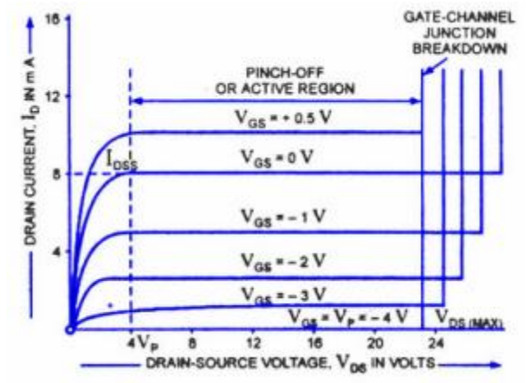


Fig.2 (ii)

It is observed that as the negative gate bias voltage V_{GS} is increased;

(1) The maximum saturation drain current becomes smaller because the conducting channel now becomes narrower.

(2) Pinch-off voltage is reached at a lower value of drain current I_D than when $V_{GS} = 0$.

When an external bias of, say – 1 V is applied between the gate and the source, the gate-channel junctions are reverse-biased even when drain current, I_D is zero. Hence the depletion regions are already penetrating the channel to a certain extent when drain-source voltage, V_{DS} is zero.

Due to this reason, a smaller voltage drop along the channel (i.e. smaller than that for $V_{GS} = 0$) will increase the depletion regions to the point where they pinch-off the current. Consequently, the pinch-off voltage V_P is reached at a lower drain current, I_D.

(3) Value of drain-source voltage V_{DS} for the avalanche breakdown of the gate junction is reduced.

It is simply due to the fact that gate-source voltage, V_{GS} keeps adding to the reverse bias at the junction produced by current flow.

Transfer Characteristic of JFET

The transfer characteristic for a JFET can be determined experimentally, keeping drain-source voltage, V_{DS} constant and determining drain current, I_D for various values of gate-source voltage, V_{GS}.

The circuit diagram is shown in fig.3 (i).

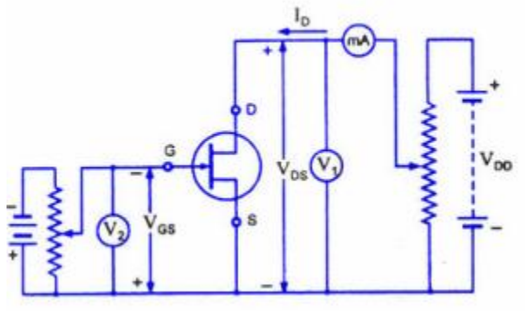


Fig.3 (i)

The curve is plotted between gate-source voltage, V_{GS} and drain current, I_D, as shown in fig. 3 (ii).

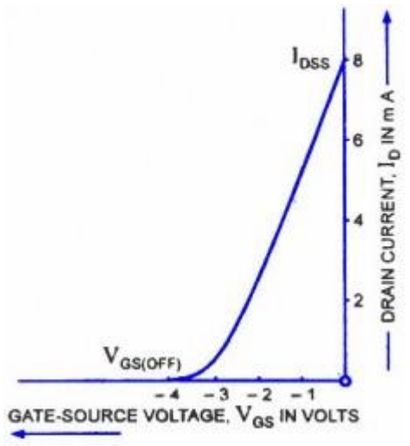


Fig.3 (ii)

It can be observed that:

(i) Drain current decreases with the increase in negative gate-source bias

(ii) Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$

(iii) Drain current, $I_D = 0$ when $V_{GS} = V_D$

The transfer characteristic can also be derived from the drain characteristic by noting values of drain current, I_D corresponding to various values of gate-source voltage, V_{GS} for a constant drain-source voltage and plotting them.

JFET Biasing

For proper operation of n-channel JFET, gate must be negative w.r.t source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

Bias Battery: In this method, JFET is biased by a bias battery V_{GG}. This battery ensures that gate is always negative w.r.t. source during all parts of the signal.

Biasing Circuit: The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. The two most commonly used methods for biasing are (i) self-bias (ii) potential divider biasing method.

JFET Biasing by Bias Battery

Fig.4 shows the biasing of a n-channel JFET by a bias battery $-V_{GG}$.

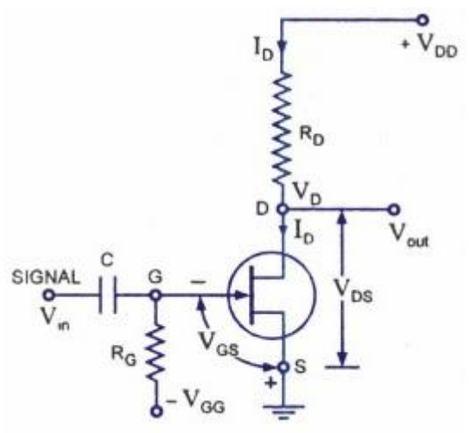


Fig.4

This method is also called gate bias. The battery voltage $-V_{GG}$ ensures that gate–source junction remains reverse biased.

Since the FET has such a high input impedance that no gate current flows, there will be no voltage drop across R_G.

Hence, $V_{GS} = V_{GG}$

We can find the value of drain current I_D from the following relation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The value of V_{DS} is given by:

$$V_{DS} = V_{DD} - I_D R_D$$

Self-Bias for JFET

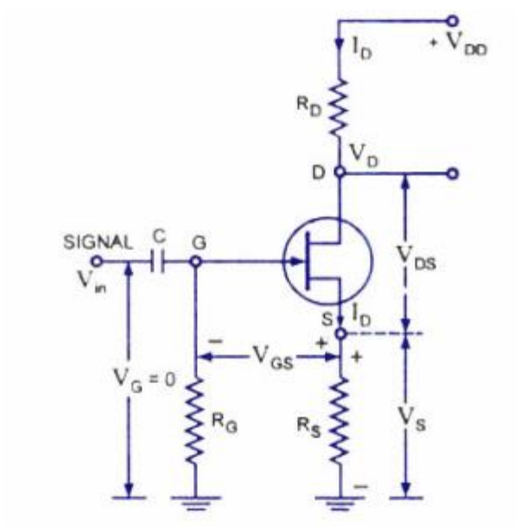


Fig.5

Fig.5 shows the self-bias method for n-channel JFET.

The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage.

Voltage across R_S, $V_S = I_D R_S$

Since gate current is negligibly small, the gate terminal is at d.c. ground i.e. $V_G = 0$

So, $V_{GS} = V_G - V_S = 0 - I_D R_S$

Or, $V_{GS} = -I_D R_S$

Thus bias voltage V_{GS} keeps gate negative w.r.t source.

The drain current I_D and drain-source voltage V_{DS} can be calculated from the following relations:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

JFET with Voltage-Divider Bias

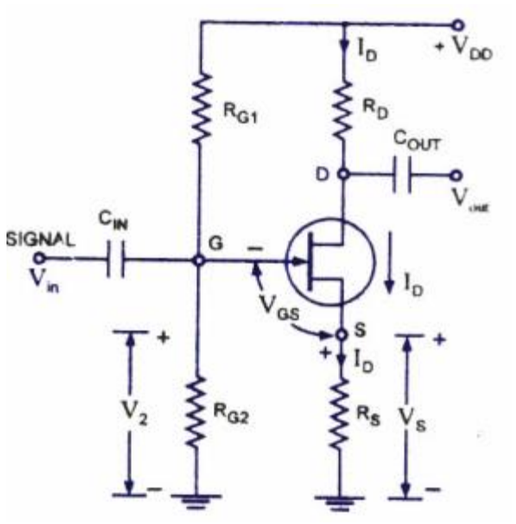


Fig.6

Fig.6 shows potential divider method of biasing a JFET.

The resistor R_1 and R_2 form a voltage divider across drain supply V_{DD}.

The voltage $V_2 = V_G$ across R_2 provides necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$V_2 = V_{GS} + I_D R_S$$

$$V_{GS} = V_2 - I_D R_S$$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the drain current and drain-source voltage as under:

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Although the circuit of voltage divider bias is a bit complex, yet the advantage of this method is that it provides good stability.

MOSFET

In case of JFET, the gate must be reverse biased for proper operation of the device i.e. it can only have negative gate operation for n-channel and positive gate operation for p-channel. That means we can only decrease the width of the channel from its zero-bias size. This type of operation is known as depletion-mode operation. Therefore, a JFET can only be operated in the depletion mode.

However, there is a field effect transistor that can be operated to enhance the width of the channel i.e. it can have enhancement-mode operation. Such a FET is called MOSFET.

Types of MOSFETs

There are two basic types of MOSFETs such as:

1. *Depletion-type MOSFET or D-MOSFET:* The D-MOSFET can be operated in both depletion mode and the enhancement mode. For this reason it is also called depletion/enhancement MOSFET.
2. *Enhancement-type MOSFET or E-MOSFET:* The E-MOSFET can be operated only in enhancement mode.

D-MOSFET

Fig.1 shows the constructional detail of n-channel D-MOSFET.

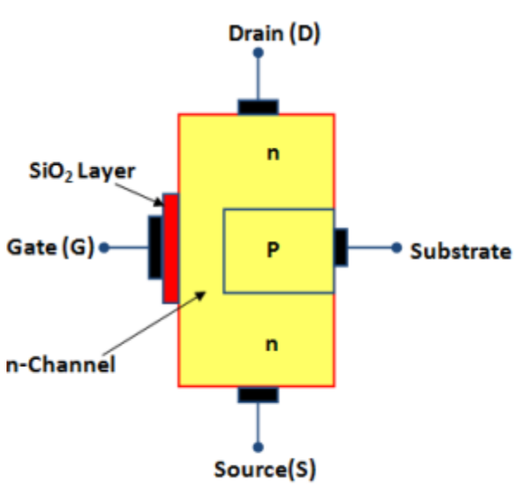


Fig.1 (n-Channel D-MOSFET)

The n-channel D-MOSFET is a piece of n-type material with a p-type region called substrate on the right and an insulated gate on the left as shown in fig.1.

The free electrons flowing from source to drain must pass through the narrow channel between the gate and the p-type region (i.e. substrate).

The gate construction of D-MOSFET is explained as below:

A thin layer of metal oxide, usually silicon dioxide (SiO2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer.

The substrate is connected to the source internally so that a MOSFET has three terminals such as Source (S), Gate (G) and Drain(D).

Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, D-MOSFET can be operated in both depletion-mode and enhancement-mode.

Symbols for D-MOSFET

There are two types of D-MOSFETs such as :

1. n-channel D-MOSFET
2. p-channel D-MOSFET

n-channel D-MOSFET

Fig.2 (i)shows the various parts of n-channel D-MOSFET.

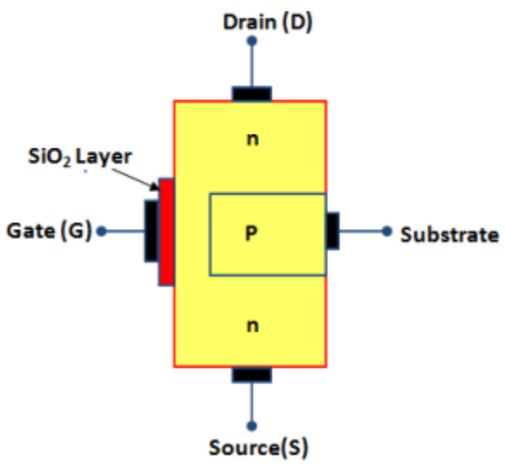


Fig.2 (i)

The p-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side.

Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel.

The symbol for n-channel D-MOSFET is shown in fig.2 (ii).

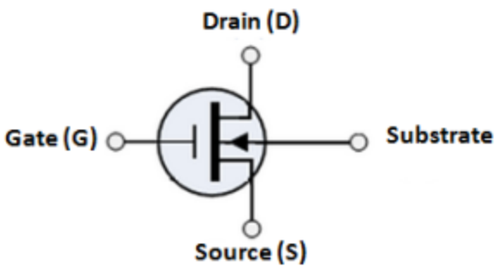


Fig.2(ii)

The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel.

The drain lead comes out of the top of the channel and the source lead connects to the bottom.

The arrow is on the substrate and points to the n-material, therefore we have nchannel D-MOSFET.

The substrate is connected to the source as shown in fig.2 (iii). This gives rise to a three terminal device.

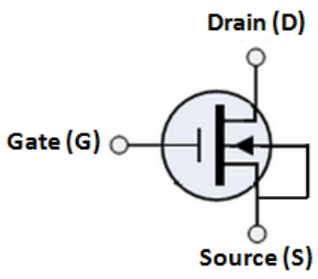


Fig.2 (iii)

p-channel D-MOSFET

Fig.3 (i) shows the various parts of p-channel D-MOSFET.

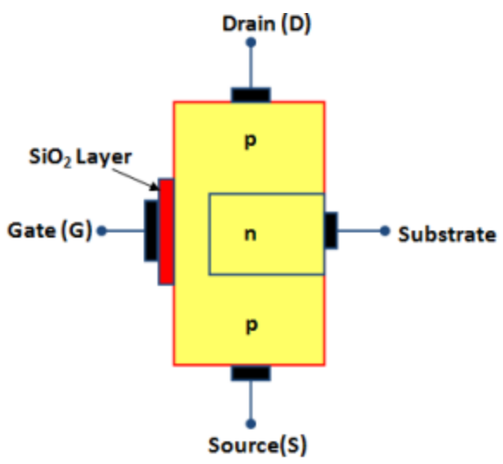


Fig.3 (i)

The n-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel.

The symbol for p-channel D-MOSFET is shown in fig.3 (ii).

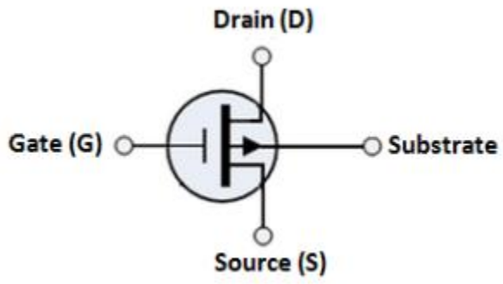


Fig.3(ii)

The source is connected to substrate internally as shown in fig.3 (iii). This results in a three-terminal device.

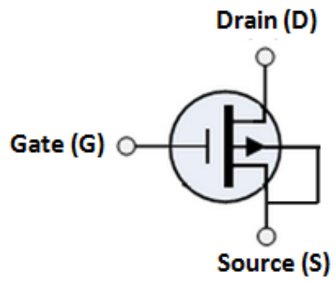


Fig.3(iii)

Circuit Operation of D-MOSFET

Fig.4 (i) shows the circuit of n-channel D-MOSFET.

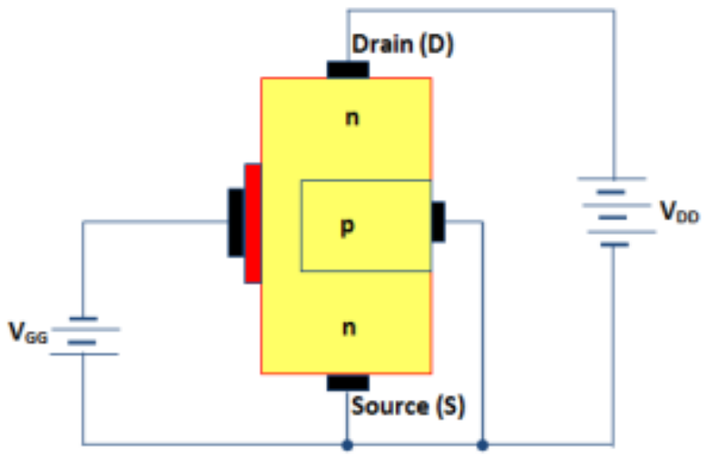


Fig.4 (i)

The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric.

When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel.

Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate.

The negative gate operation is called *depletion mode* and positive gate operation is called *enhancement mode*.

1. **Depletion mode:**

Fig.5 (i) shows depletion mode operation of n-channel D-MOSFET.

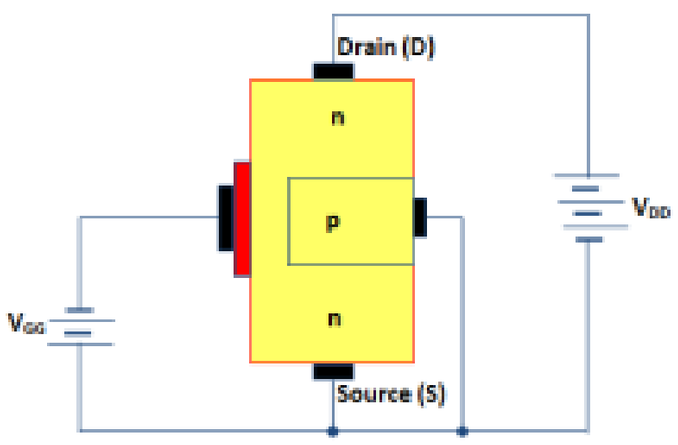


Fig.5 (i)

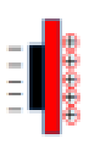


Fig.5 (ii)

Since gate is negative, it means electrons are on the gate as shown in fig.5 (ii).

These electrons repel the free electrons in the n-channel, leaving a layer of positive ions in a part of the channel as shown in fig.5 (ii).In other words, the n-channel is depleted of some of its free electrons.

Therefore, lesser number of free electrons are available for current conduction through the n-channel. This is same as increasing the channel resistance.

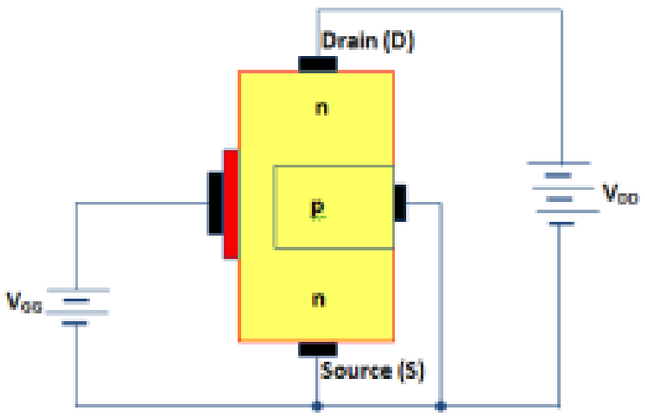
The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the n-channel and hence the current from source to drain.

As the action with negative gate depends upon depleting the channel of free electrons, the negative-gate operation is called depletion mode.

2. **Enhancement mode:**

Fig.6 (i) shows enhancement mode operation of n-channel D-MOSFET.



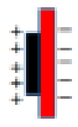


Fig.6 (i) Fig.6 (ii)

Again the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the n-channel as shown in fig.6 (ii).

These negative charges are the free electrons drawn into the channel.

Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased.

Thus a positive gate voltage enhances or increases the conductivity of the channel.

The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel.

Because the action with a positive gate depends upon enhancing the conductivity of the channel, the positive gate operation is called enhancement mode.

The following points may be noted about D-MOSFET operation:

1. In a D-MOSFET, the source to drain current is controlled by the electric field of capacitor formed at the gate.
2. The gate of a D-MOSFET acts like a capacitor. For this reason it is possible to operate D-MOSFET with positive or negative gate voltage.
3. As the gate of D-MOSFET forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate. For this reason, the input impedance of D-MOSFET is very high ranging from 10,000 MΩ to 10,000,00 MΩ.
4. The extremely small dimensions of oxide layer under the gate terminal results is a very low capacitance and the D-MOSFET has, therefore, a very low input capacitance. This characteristics makes the D-MOSFET useful in high frequency applications.

E-MOSFET

Fig.7 shows the constructional details of n-channel E-MOSFET.

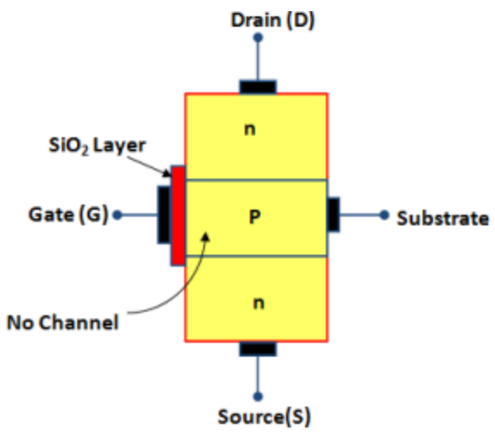


Fig.7

Its gate construction is similar to that of D-MOSFET.

The E-MOSFET has no channel between source and drain. The substrate extends completely to the SiO2 layer so that no channel exists.

The E-MOSFET requires a proper gate voltage to form a channel , called induced channel between the source and the drain.

It operates only in the enhancement mode and has no depletion mode.

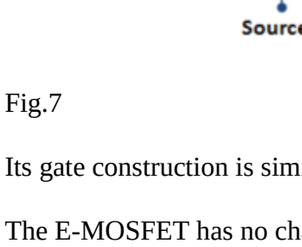
Only by applying V_{GS} of proper magnitude and polarity, the device starts conducting.

The minimum value of V_{GS} of proper polarity that turns on the E-MOSFET is called *threshold voltage* [$V_{GS(th)}$].

The n-channel device requires positive V_{GS} ($\geq V_{GS(th)}$) and the p-channel device requires negative V_{GS}($\geq V_{GS(th)}$).

Symbols for E-MOSFET

Fig.8 (i) shows the schematic symbols for n-channel E-MOSFET and Fig.8 (ii) shows the schematic symbol for p-channel E-MOSFET.



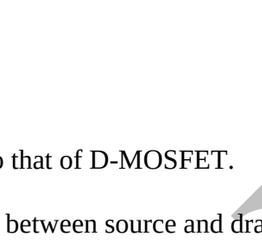


Fig.8 (i) Fig.8 (ii)

Circuit Operation of E-MOSFET

Fig.9 (i) shows the circuit of n-channel E-MOSFE. The circuit action is as under:

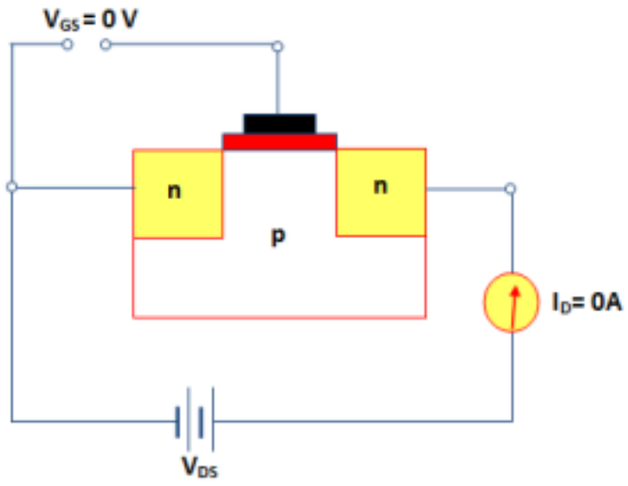


Fig.9 (i)

(i) **When V_{GS}= 0V,** as shown in fig.9 (i), there is no channel connecting source and drain.

The p-substrate has only a few thermally produced free electrons(minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when V_{GS} = 0V.

(ii) **When V_{GS} is positive**, i.e gate is made positive as shown in fig.9(ii), it attracts free electrons into the p region. The free electrons combine with the holes next to the SiO2 layer.

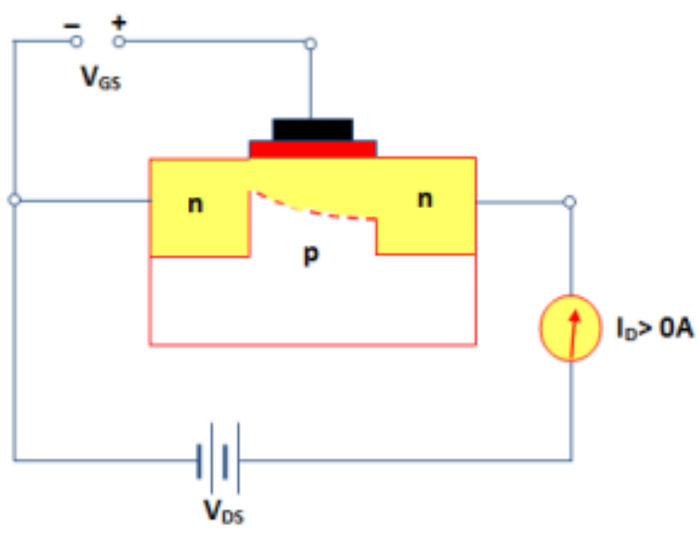


Fig.9 (ii)

If V_{GS} is positive enough, all the holes touching the SiO2 layer are filled and free electrons begin to flow from the source to drain.

The effect is same as creating a thin layer of n-type material i.e. inducing a thin n-layer adjacent to the SiO2 layer.

Thus the E-MOSFET is turned ON and drain current I_D starts flowing from the source to the drain.

The minimum value of V_{GS} that turns the E-MOSFET ON is called threshold voltage[$V_{GS(th)}$].

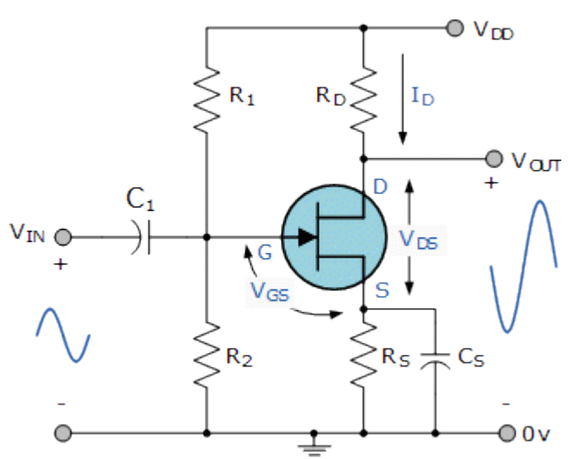
(iii) **When V_{GS} is less than $V_{GS(th)}$,** there is no induced channel and the drain current $I_D$is zero.

When V_{GS} is equal to $V_{GS(th)}$, the E-MOSFET is turned ON and the induced channel conducts drain current from the source to the drain.

Beyond $V_{GS(th)}$, if the value of V_{GS} is increased,the newly formed channel becomes wider, causing to I_D to increase.

If the value of V_{GS} decreases not less than $V_{GS(th)}$, the channel becomes narrower and I_D will decrease.

Common Source JFET Amplifier



Transistor amplifier circuits such as the common emitter amplifier are made using Bipolar Transistors, but small signal amplifiers can also be made using Field Effect Transistors. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals.

The design of an amplifier circuit based around a junction field effect transistor or “JFET”, (N-channel FET for this tutorial) or even a metal oxide silicon FET or “MOSFET” is exactly the same principle as that for the bipolar transistor circuit used for a Class A amplifier circuit we looked at in the previous tutorial.

Firstly, a suitable quiescent point or “Q-point” needs to be found for the correct biasing of the JFET amplifier circuit with single amplifier configurations of Common-source (CS), Common-drain (CD) or Source-follower (SF) and the Common-gate (CG) available for most FET devices.

These three JFET amplifier configurations correspond to the common-emitter, emitter-follower and the common-base configurations using bipolar transistors. In this tutorial about FET amplifiers we will look at the popular **Common Source JFET Amplifier** as this is the most widely used JFET amplifier design.

The amplifier circuit consists of an N-channel JFET, but the device could also be an equivalent N-channel depletion-mode MOSFET as the circuit diagram would be the same just a change in the FET, connected in a common source configuration. The JFET gate voltage Vg is biased through the potential divider network set up by resistors R1 and R2 and is biased to operate within its saturation region which is equivalent to the active region of the bipolar junction transistor.

Unlike a bipolar transistor circuit, the junction FET takes virtually no input gate current allowing the gate to be treated as an open circuit. Then no input characteristics curves are required

Since the N-Channel JFET is a depletion mode device and is normally “ON”, a negative gate voltage with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by biasing from a separate power supply voltage or by a self biasing arrangement as long as a steady current flows through the JFET even when there is no input signal present and Vg maintains a reverse bias of the gate-source pn junction.

In our simple example, the biasing is provided from a potential divider network allowing the input signal to produce a voltage fall at the gate as well as voltage rise at the gate with a sinusoidal signal. Any suitable pair of resistor values in the correct proportions would produce the correct biasing voltage so the DC gate biasing voltage Vg is given as:

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this equation only determines the ratio of the resistors R1 and R2, but in order to take advantage of the very high input impedance of the JFET as well as reducing the power dissipation within the circuit, we need to make these resistor values as high as possible, with values in the order of 1MΩ to 10MΩ being common.

The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, Rd. The output voltage, Vout is developed across this load resistance.

The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, Rs included in the source lead with the same drain current flowing through this resistor. Resistor, Rs is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to Rs*Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$V_S = I_D \times R_S = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as "No Current" enters the Gate terminal and this can be given as:

$$I_D = \frac{V_S}{R_S} = \frac{V_{DD}}{R_D + R_S}$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, Rs and the source by-pass capacitor, Cs serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped across Rs.

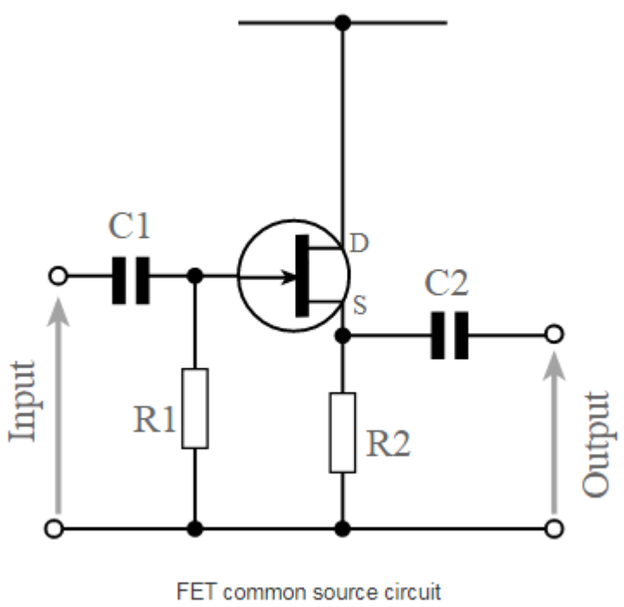
The the value in farads of the source by-pass capacitor is generally fairly high above 100uF and will be polarized. This gives the capacitor an impedance value much smaller, less than 10% of the transconductance, gm (the transfer coefficient representing gain) value of the device. At high frequencies the by-pass capacitor acts essentially as a short-circuit and the source will be effectively connected directly to ground.

The basic circuit and characteristics of a **Common Source JFET Amplifier** are very similar to that of the common emitter amplifier. A DC load line is constructed by joining the two points relating to the drain current, Id and the supply voltage, Vdd remembering that when Id = 0: (Vdd = Vds) and when Vds = 0: (Id = Vdd/R_L).

Common Drain Amplifier

The typical implementation of the common drain or source follower / buffer circuit is very easy to realise in a practical fashion.

The circuit show below gives a typical example of a FET source follower / buffer circuit. The capacitors C1 and C2 are used to couple the AC signal between stages and block the DC elements. The resistor R1 provides the gate bias, holding he gate at ground potential. The source circuit shows the resistor R2 to ground - its value is determined by the channel current that is required.



FET common source circuit

The source follower circuit presents a very high impedance to the preceding stage and it is for this reason that the source follower is an ideal format for use as a buffer.

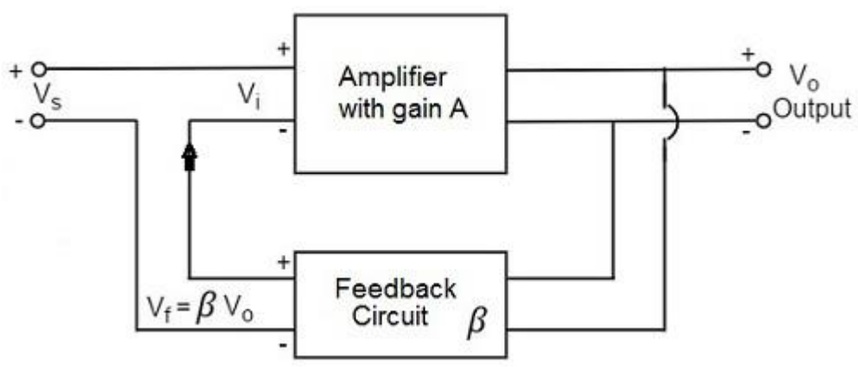
Feedback

An amplifier circuit simply increases the signal strength. But while amplifying, it just increases the strength of its input signal whether it contains information or some noise along with information. This noise or some disturbance is introduced in the amplifiers because of their strong tendency to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output, which is very undesirable.

The noise level in the amplifier circuits can be considerably reduced by using negative feedback done by injecting a fraction of output in phase opposition to the input signal.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure.



From the above figure, the gain of the amplifier is represented as A. the gain of the amplifier is the ratio of output voltage V_o to the input voltage V_i. the feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s. Now,

Vi=Vs+Vf=Vs+βVoVi=Vs+Vf=Vs+βVo

Vi=Vs−Vf=Vs−βVoVi=Vs−Vf=Vs−βVo

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

Let us consider the case of negative feedback. The output V_o must be equal to the input voltage (V_s - βV_o) multiplied by the gain A of the amplifier.

Hence,

$(Vs-\beta Vo)A=Vo(Vs-\beta Vo)A=Vo$

Or

$AVs-A\beta Vo=VoAVs-A\beta Vo=Vo$

Or

$AVs=Vo(1+A\beta)AVs=Vo(1+A\beta)$

Therefore,

$VoVs=A1+A\beta VoVs=A1+A\beta$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

$Af=OutputvoltageInputsignalvoltage=VoVsAf=OutputvoltageInputsignalvoltage=VoVs$

So, from the above two equations, we can understand that,

The equation of gain of the feedback amplifier, with negative feedback is given by

$Af=A1+A\beta Af=A1+A\beta$

The equation of gain of the feedback amplifier, with positive feedback is given by

$Af=A1-A\beta Af=A1-A\beta$

These are the standard equations to calculate the gain of feedback amplifiers.

Types of Feedbacks

The process of injecting a fraction of output energy of some device back to the input is known as Feedback. It has been found that feedback is very useful in reducing noise and making the amplifier operation stable.

Depending upon whether the feedback signal aids or opposes the input signal, there are two types of feedbacks used.

Positive Feedback

The feedback in which the feedback energy i.e., either voltage or current is in phase with the input signal and thus aids it is called as Positive feedback.

Both the input signal and feedback signal introduces a phase shift of 180^o thus making a 360^o resultant phase shift around the loop, to be finally in phase with the input signal.

Though the positive feedback increases the gain of the amplifier, it has the disadvantages such as

- Increasing distortion
- Instability

It is because of these disadvantages the positive feedback is not recommended for the amplifiers. If the positive feedback is sufficiently large, it leads to oscillations, by which oscillator circuits are formed. This concept will be discussed in OSCILLATORS tutorial.

Negative Feedback

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as negative feedback.

In negative feedback, the amplifier introduces a phase shift of 180^o into the circuit while the feedback network is so designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage V_f is 180^o out of phase with the input signal V_{in}.

Though the gain of negative feedback amplifier is reduced, there are many advantages of negative feedback such as

- Stability of gain is improved
- Reduction in distortion
- Reduction in noise
- Increase in input impedance
- Decrease in output impedance
- Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

Negative feedback in an amplifier is the method of feeding a portion of the amplified output to the input but in opposite phase. The phase opposition occurs as the amplifier provides 180^o phase shift whereas the feedback network doesn't.

While the output energy is being applied to the input, for the voltage energy to be taken as feedback, the output is taken in shunt connection and for the current energy to be taken as feedback, the output is taken in series connection.

There are two main types of negative feedback circuits. They are −

- Negative Voltage Feedback
- Negative Current Feedback

Negative Voltage Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output voltage. This is further classified into two types −

- Voltage-series feedback
- Voltage-shunt feedback

Negative Current Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output current. This is further classified into two types.

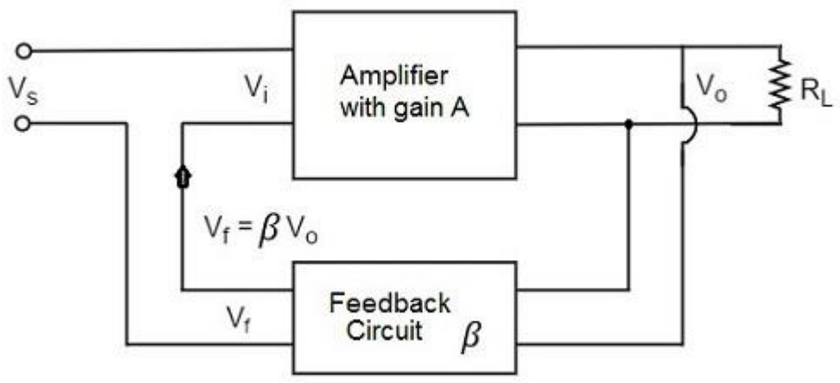
- Current-series feedback
- Current-shunt feedback

Let us have a brief idea on all of them.

Voltage-Series Feedback

In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as **shunt-driven series-fed** feedback, i.e., a parallel-series circuit.

The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.

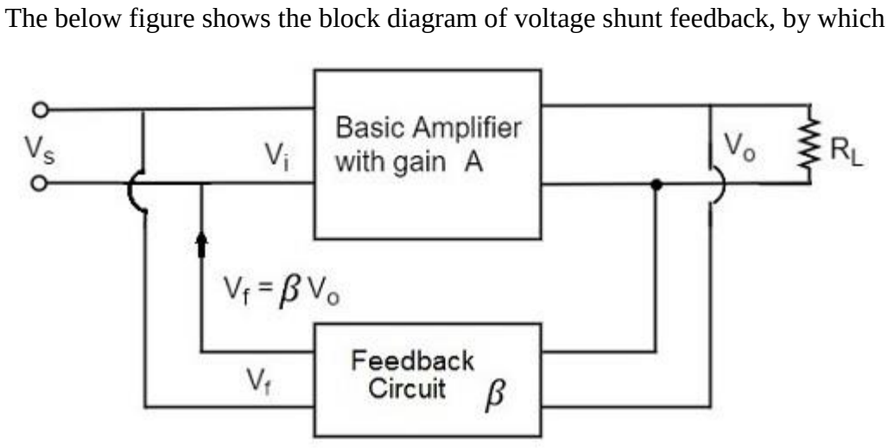


As the feedback circuit is connected in shunt with the output, the output impedance is decreased and due to the series connection with the input, the input impedance is increased.

Voltage-Shunt Feedback

In the voltage shunt feedback circuit, a fraction of the output voltage is applied in parallel with the input voltage through the feedback network. This is also known as **shunt-driven shunt-fed** feedback i.e., a parallel-parallel proto type.

The below figure shows the block diagram of voltage shunt feedback, by which it is evident that the feedback circuit is placed in shunt with the output and also with the input.

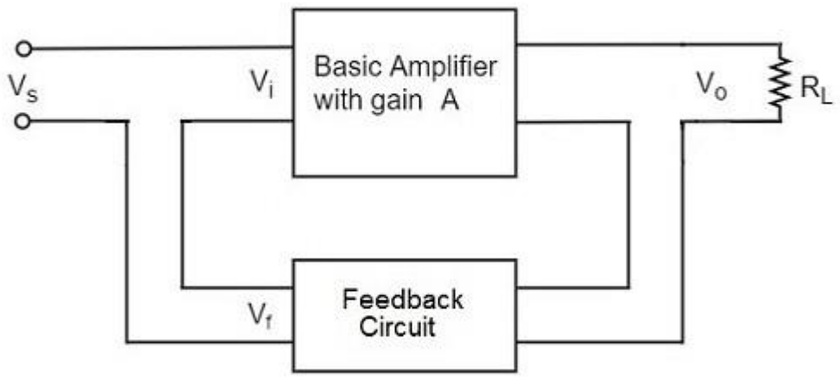


As the feedback circuit is connected in shunt with the output and the input as well, both the output impedance and the input impedance are decreased.

Current-Series Feedback

In the current series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as **series-driven series-fed** feedback i.e., a series-series circuit.

The following figure shows the block diagram of current series feedback, by which it is evident that the feedback circuit is placed in series with the output and also with the input.

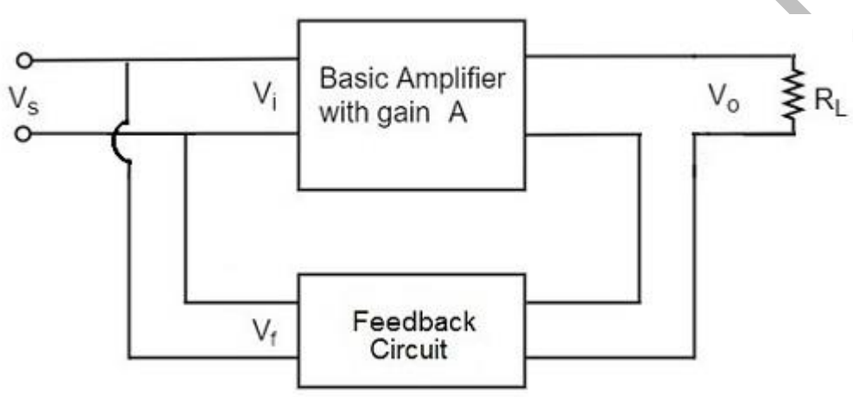


As the feedback circuit is connected in series with the output and the input as well, both the output impedance and the input impedance are increased.

Current-Shunt Feedback

In the current shunt feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as **series-driven shunt-fed** feedback i.e., a series-parallel circuit.

The below figure shows the block diagram of current shunt feedback, by which it is evident that the feedback circuit is placed in series with the output but in parallel with the input.



As the feedback circuit is connected in series with the output, the output impedance is increased and due to the parallel connection with the input, the input impedance is decreased.

MODULE 4

POWER AMPLIFIERS

- Not all amplifiers are the same and there is a clear distinction made between the way their output stages are configured and operate.
- The main operating characteristics of an ideal amplifier are linearity, signal gain, efficiency and power output but in real world amplifiers there is always a trade off between these different characteristics.
- Generally, large signal or power amplifiers are used in the output stages of audio amplifier systems to drive a loudspeaker load.
- A typical loudspeaker has an impedance of between 4Ω and 8Ω, thus a power amplifier must be able to supply the high peak currents required to drive the low impedance speaker.

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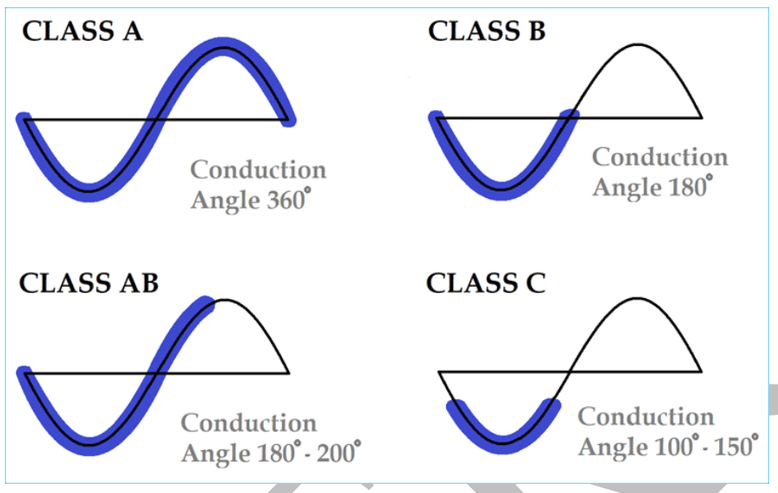
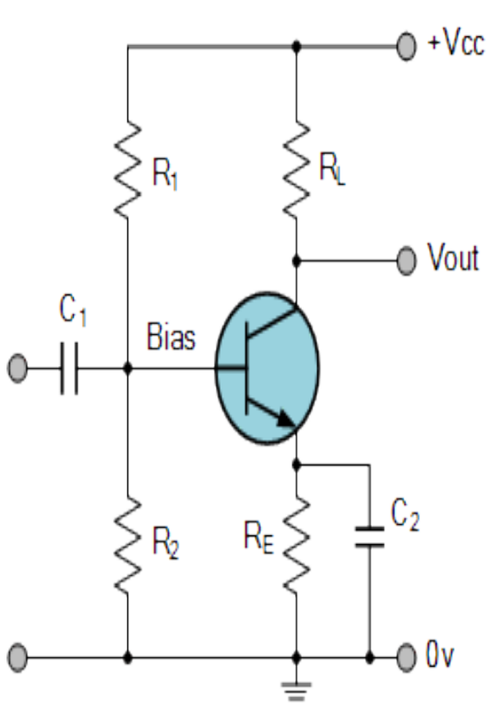
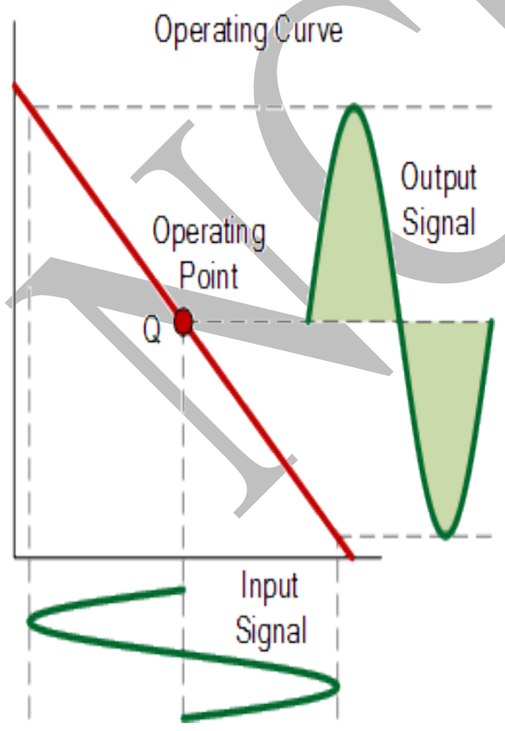


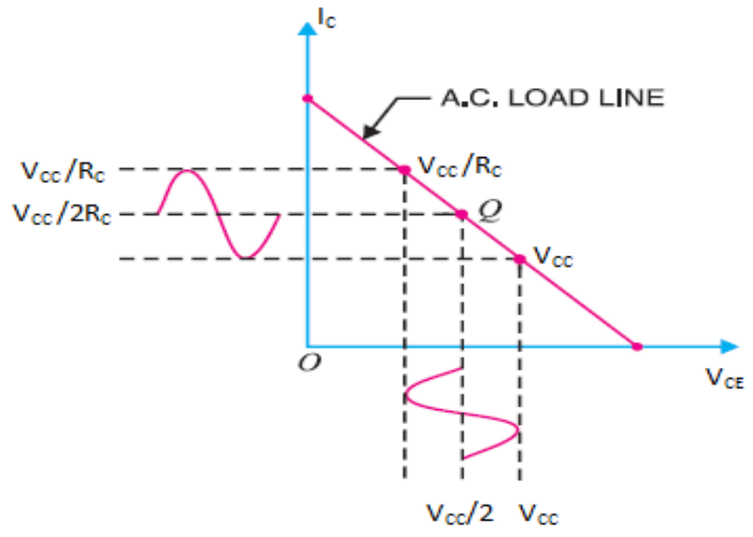
CLASS A POWER AMPLIFIER

DIRECTLY COUPLED OR SERIES FED CLASS A POWER AMPLIFER





- To achieve high linearity and gain, the output stage of a class A amplifier is biased “ON” (conducting) all the time.
- Then for an amplifier to be classified as “Class A” the zero signal idle current in the output stage must be equal to or greater than the maximum load current (usually a loudspeaker) required to produce the largest output signal.
- As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform.
- Then the class A amplifier is equivalent to a current source.
- Since a class A amplifier operates in the linear region, the transistors base (or gate) DC biasing voltage should by chosen properly to ensure correct operation and low distortion.
- However, as the output device is “ON” at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier.
- Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30%, making them impractical for high-power amplifications.
- Also due to the high idling current of the amplifier, the power supply must be sized accordingly and be well filtered to avoid any amplifier hum and noise.
- Therefore, due to the low efficiency and over heating problems of Class A amplifiers, more efficient amplifier classes have been developed.



D.C. Power drawn from collector battery V_{cc} is given by

$$P_{in} = voltage \times current = V_{CC}(I_C)_Q$$

This power is used in the following two parts –

- Power dissipated in the collector load as heat is given by

$$P_{RC} = (current)^2 \times resistance = (I_C)_Q^2 R_C$$

- Power given to transistor is given by

$$P_{tr} = P_{in} - P_{RC} = V_{CC} - (I_C)_Q^2 R_C$$

When signal is applied, the power given to transistor is used in the following two parts –

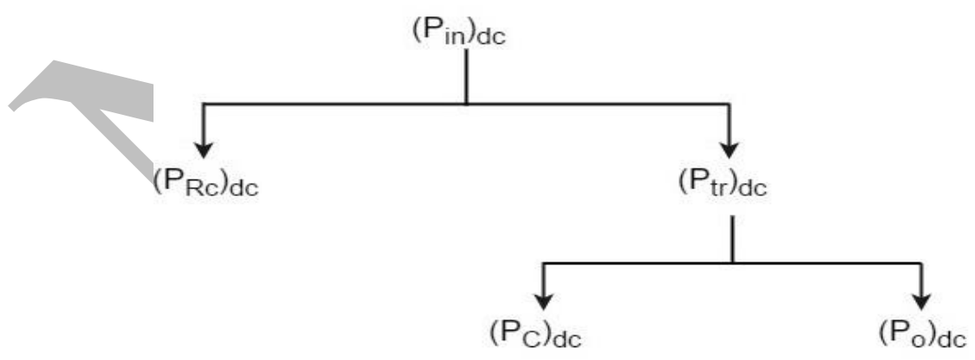
- A.C. Power developed across load resistors RC which constitutes the a.c. power output.

$$(P_O)_{ac} = I^2 R_C = \frac{V^2}{R_C} = \left(\frac{V_m}{\sqrt{2}}\right)^2 \frac{1}{R_C} = \frac{V_m^2}{2R_C}$$

Where **I** is the R.M.S. value of a.c. output current through load, **V** is the R.M.S. value of a.c. voltage, and $\mathbf{V_m}$ is the maximum value of V.

- The D.C. power dissipated by the transistor (collector region) in the form of heat, i.e., $(P_C)_{dc}$

We have represented the whole power flow in the following diagram.



Efficiency of Directly coupled Class A power amp

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$(\eta)_{overall} = \frac{a.c\ power\ delivered\ to\ the\ load}{total\ power\ delivered\ by\ d.c\ supply}$$

$$= \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$(\eta)_{collector} = \frac{average\ a.c\ power\ output}{average\ d.c\ power\ input\ to\ transistor}$$

$$= \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Expression for overall efficiency

$$(P_O)_{ac} = V_{rms} \times I_{rms}$$

$$(P_O)_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] \times \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right]$$

$$= \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8}$$

Therefore

$$(\eta)_{overall} = \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8 \times V_{CC}(I_C)_Q}$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows −

- The current flows for complete input cycle
- It can amplify small signals
- The output is same as input
- No distortion is present

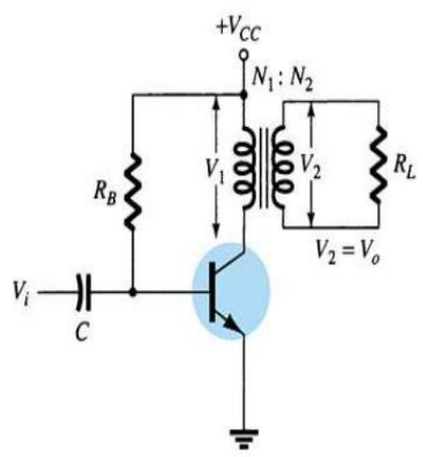
Disadvantages of Class A Amplifiers

The disadvantages of Class A power amplifier are as follows

- Low power output
- Low collector efficiency

Transformer-Coupled Class A Amplifier

This circuit uses a transformer to couple to the load. This improves the efficiency of the Class A to 50%.



Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(P_{in})_{dc} = (P_{tr})_{dc} = V_{CC} \times (I_C)_Q$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_c)_{max}$ to zero.

Hence

$$V_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max}}{2}\right] = \frac{2V_{CC}}{2\sqrt{2}} = \frac{V_{CC}}{\sqrt{2}}$$

$$I_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max}}{2}\right] = \frac{2(I_C)_Q}{2\sqrt{2}} = \frac{(I_C)_Q}{\sqrt{2}}$$

Therefore,

$$(P_O)_{ac} = V_{rms} \times I_{rms} = \frac{V_{CC}}{\sqrt{2}} \times \frac{(I_C)_Q}{\sqrt{2}} = \frac{V_{CC} \times (I_C)_Q}{2}$$

Therefore,

$$\text{Collector Efficiency} = \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Or,

$$(\eta)_{collector} = \frac{V_{CC} \times (I_C)_Q}{2 \times V_{CC} \times (I_C)_Q} = \frac{1}{2}$$

$$= \frac{1}{2} \times 100 = 50\%$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

- No loss of signal power in the base or collector resistors.
- Excellent impedance matching is achieved.
- Gain is high.
- DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

- Low frequency signals are less amplified comparatively.
- Hum noise is introduced by transformers.
- Transformers are bulky and costly.
- Poor frequency response.

Class B Power Amplifiers

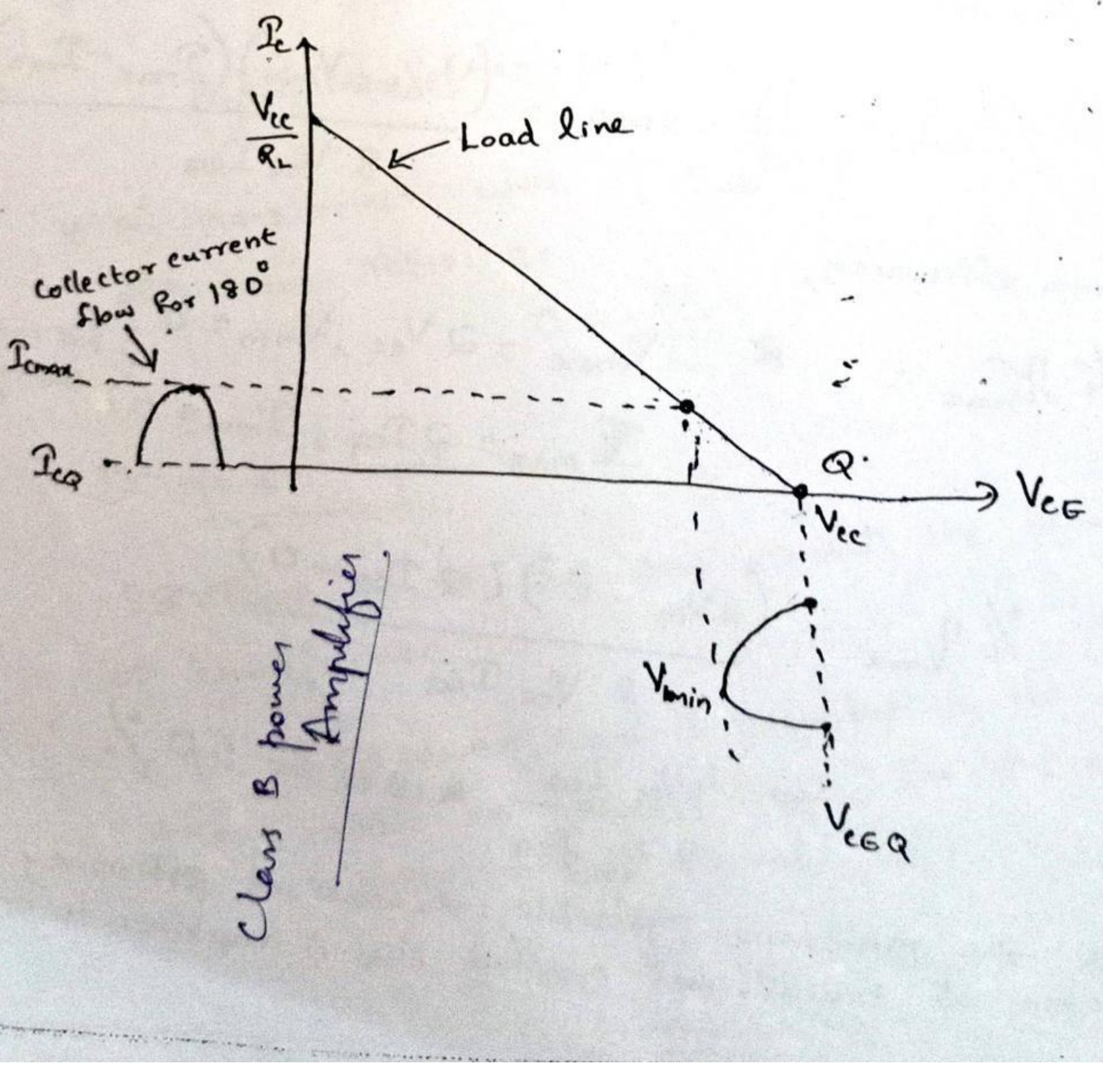
* For this operation, the Q-point is shifted on X-axis, ie. transistor is biased to cut off.

* Due to the selection of Q-point on the X-axis, the transistor remains, in the active region only for the positive half cycle of the input signal.

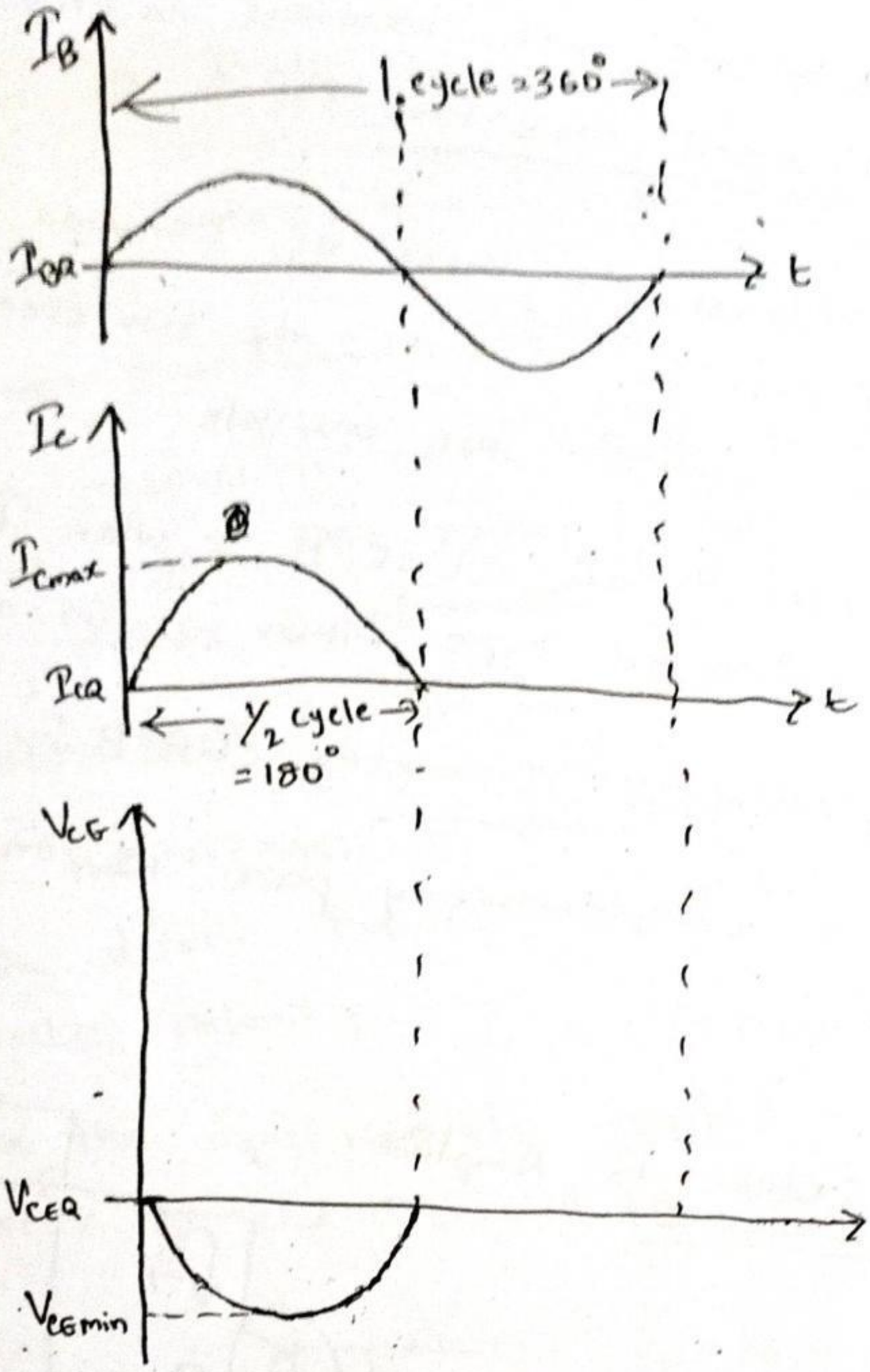
* Hence this half cycle is reproduced at the output.

* But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no-signal is produced at the output.

* The collector current flows only for 180° (half cycle) of the input signal.



Class B power Amplifier



Analysis of Class B Amplifiers

* Due to this collector current flows only for a half cycle for a full cycle of the input signal
* Hence the output signal is distorted.
* To get Full cycle across the load, a pair of transistors is used in class B operation.
* The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained.

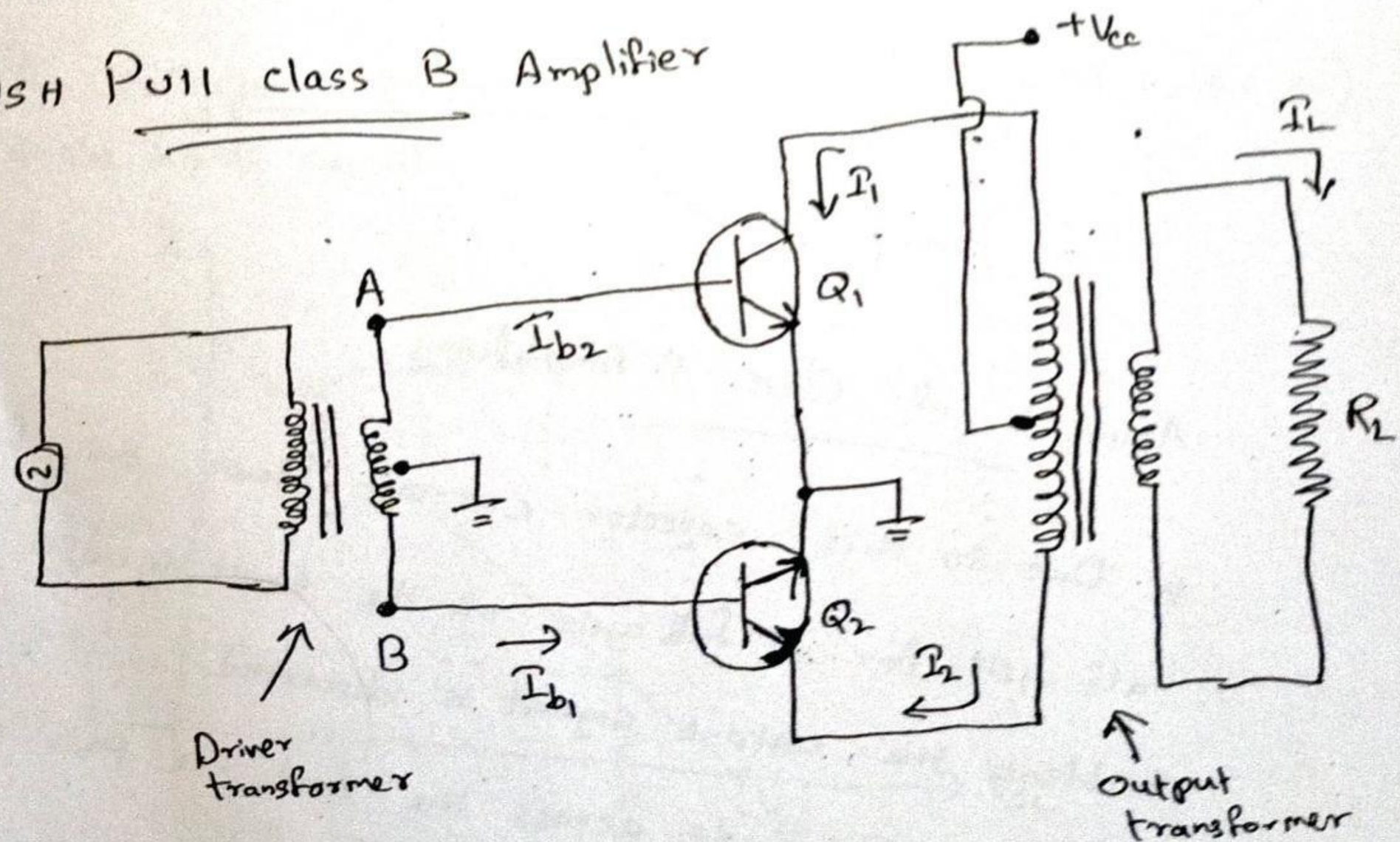
* The two transistors are identical in characteristics and called matched transistors.

* Depending upon the types of the two transistors whether P-N-P or N-P-N, the two circuit configurations of class B amplifiers are possible.

① Push Pull class B :- when two transistors are of same type either N-P-N or P-N-P.

② Complementary Symmetry class B :- Two transistors form a complementary pair. ie. one N-P-N and other P-N-P.

PUSH PULL class B Amplifier



→ Push pull circuit requires two transformer
① Input transformer (Driver transformer)
② Output transformer

→ Both transformers are centre tapped.

→ Both Q_1 & Q_2 are n-p-n

→ Both transistors are in Common Emitter Configuration

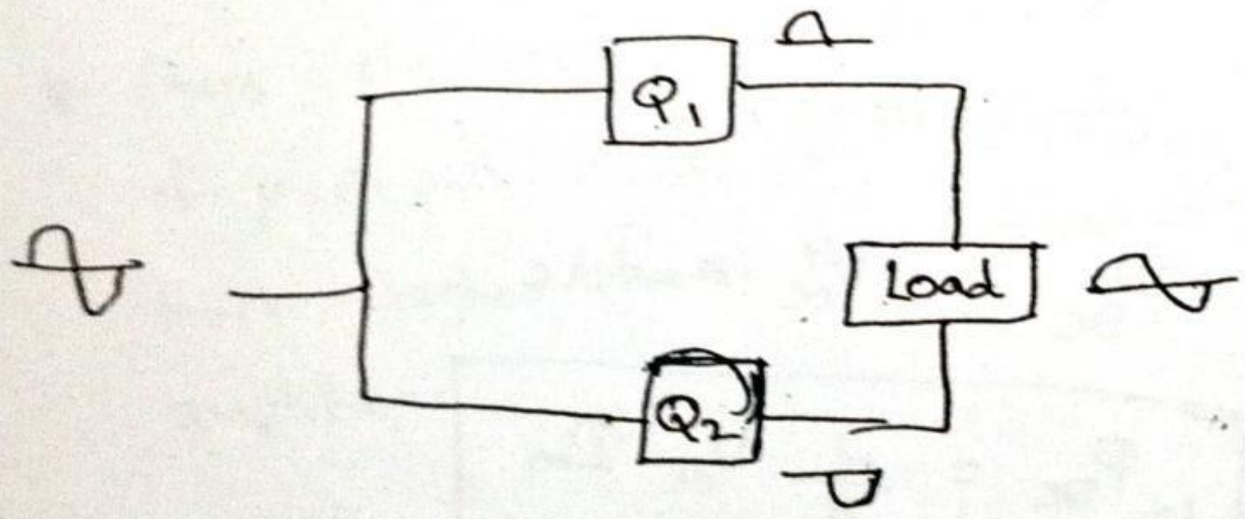
→ Driver transformer drives the circuit.

* With respect to centre tap, for a positive halfcycle of input signal, the point A shown on the secondary of the driver transformer will be positive.

* While point B, will be negative.

* Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity.

* Hence the input signals applied to the base of the transistor Q_1 and Q_2 will be 180° out of phase.



* The transistor Q_1 conducts for the positive halfcycle of the input producing positive half cycle across the load.

* Transistor Q_2 conducts for negative half cycle of the input producing negative halfcycle across the load; We get a full cycle on the load.

* when point A is positive, transistor Q_1 get driven into an active region while the transistor Q_2 is in cut-off region.

* while point A is negative, Point B is positive hence the transistor Q_2 is in active region, while the transistor Q_1 is in cut-off region.

DC power input

* The two currents drawn by the two transistor, form the d.c supply are in the same direction.

* Hence the total d.c or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$$

Total d.c power input,

$$P_{DC} = V_{cc} \times I_{dc}$$

$$\boxed{P_{DC} = \frac{2}{\pi} V_{cc} I_m}$$

AC power output

* I_m & V_m are the peak values or maximum values of the output current & output voltage respectively, then

$$\boxed{P_{ac} = \frac{V_m I_m}{2}}$$

Efficiency of Class B amplifier

$$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100$$

$$= \frac{\frac{V_m I_m}{2}}{\frac{2}{\pi} V_{cc} I_m} \times 100$$

$$\% \eta = \frac{\pi}{4} \frac{V_m}{V_{cc}} \times 100$$

maximum efficiency,

$V_m = V_{cc}$ for maximum η

$$\% \eta_{max} = \frac{\pi}{4} \times \frac{V_{cc}}{V_{cc}} \times 100$$

$$= 78.5\ \%$$

* Thus the maximum possible theoritical efficiency of push pull class B amplifier is 78.5 % which is much higher than the transformer coupled class A amplifier.

(2) Complementary Symmetry Class B Amplifier

* Instead of using same type of transistors, one n-p-n & other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier.

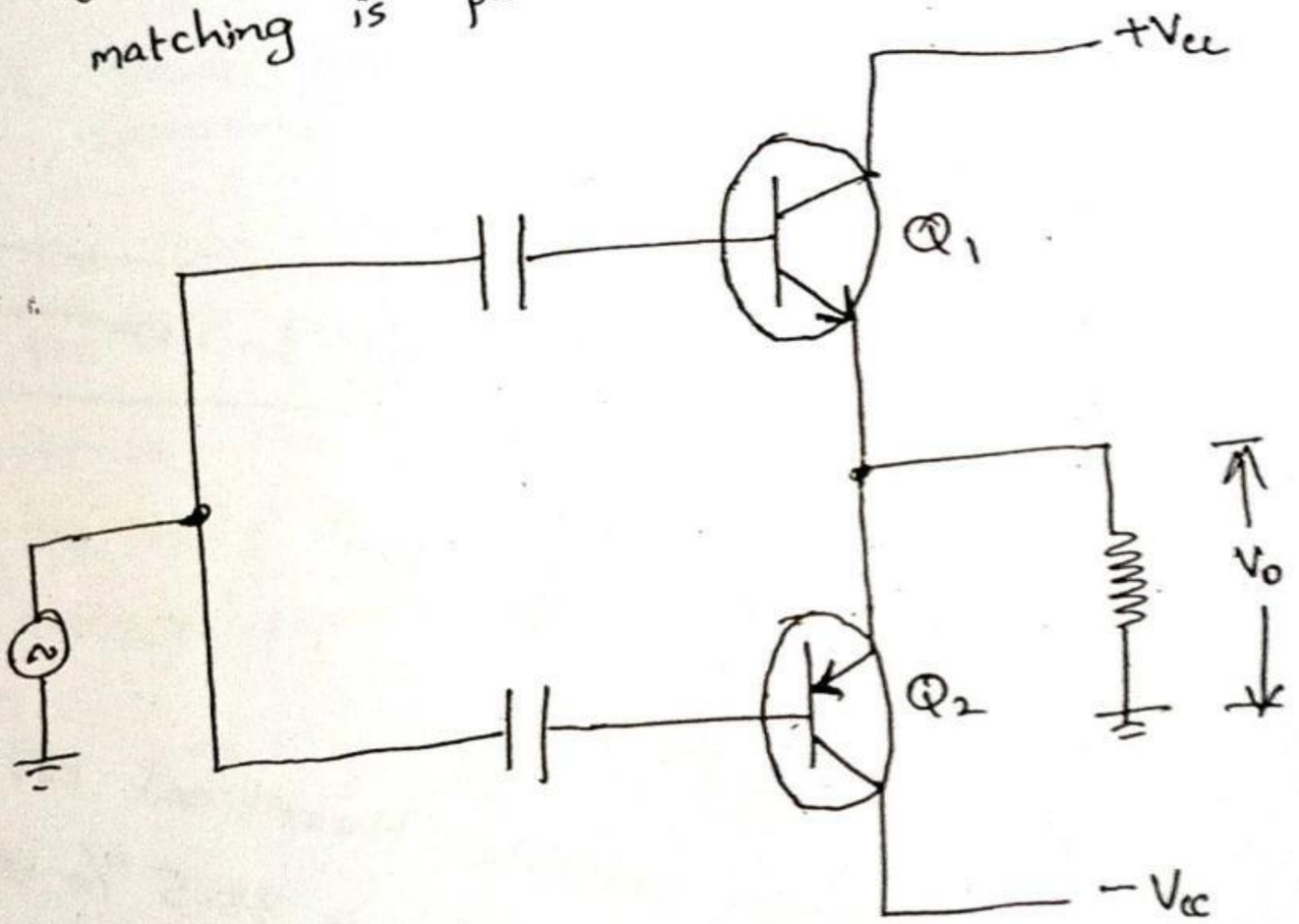
* This circuit is transformer less circuit.

* But with common emitter configuration it becomes difficult to match the output impedance for

maximum power transfer without an output transformer

* Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration in this circuit.

→ This is because common collector configurations has lowest output impedance and hence the impedance matching is possible.



* During positive half cycle, transistor Q_1 gets driven into active region & Q_2 in cut-off region.

* During Negative half cycle, transistor Q_1 will be in cut-off region & Q_2 is in active region.

* Thus a complete cycle of output signal is developed across the load.

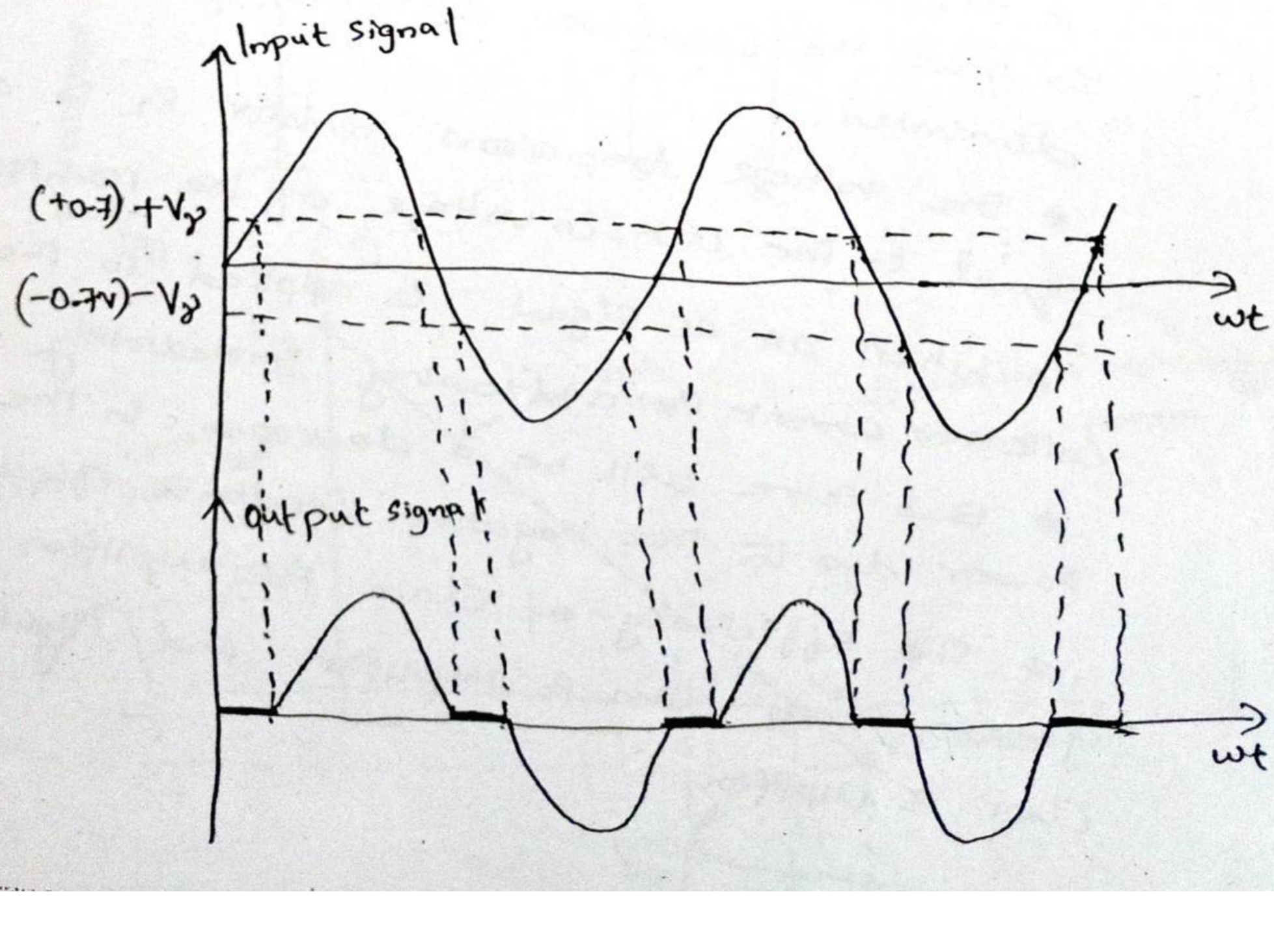
For students

Mathematical Analysis

All the results derived for push pull transformer coupled class B amplifier are applicable to the complementary class B amplifier

Cross over distortion

* For a transistor to be in active region the base emitter junction must be forward biased.
* The junction cannot be made forward biased till the voltage applied becomes greater than cut-in voltage (V_γ) of the junction, which is generally 0.7 V for silicon and 0.3 V for germanium transistors.
* Hence as long as the magnitude of the input signal is less than the cut in voltage of the base-emitter junction, the collector current remains zero and transistor remains in cut-off region.
* Hence the nature of the output signal gets distorted and no longer remains same as that of input.
* Such a distortion in the output signal is called cross over distortion.



Class AB amplifier:

* It overcomes the problem of crossover distortion in class B amplifiers, in which a small current flows even at zero input signal level.

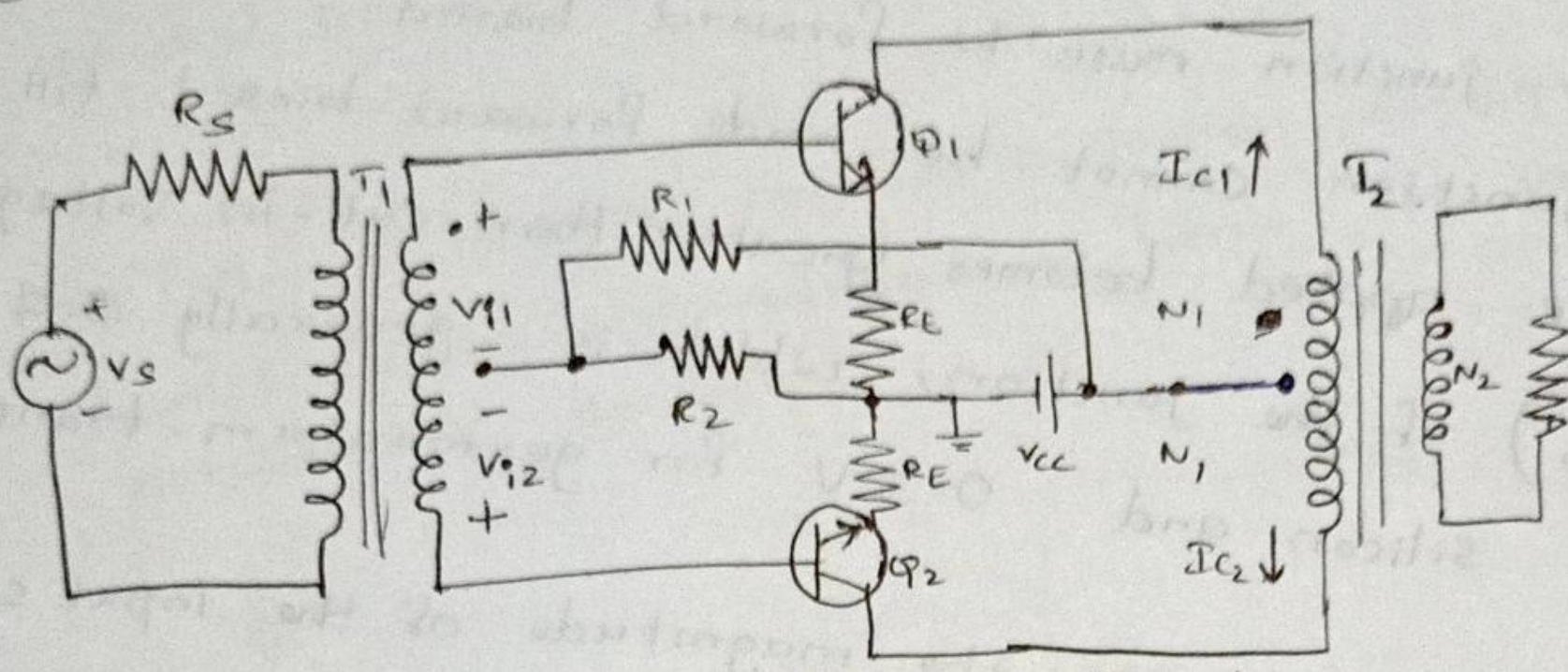


Fig: Class AB amplifier.

* The circuit, which is essentially the same as that of class B amplifier, has additional R_E resistors refferred to as the emitter stabilizing resistor.

* This biases the transistor away from class B amplifier slightly towards class A operation.

* The transistors Q_1 and Q_2 are biased such that the Q point of class AB is placed inbetween the active region of class A and cut-off region of class B.

* The transistors therefore conduct for more than 180°, so that the cross over distortion present in class B is diminated.

* The voltage drop across resistor R_2 is approximately equal to the cut-in voltage of the transistor

* When an ac signal is applied to the base, the collector current starts flowing immediately

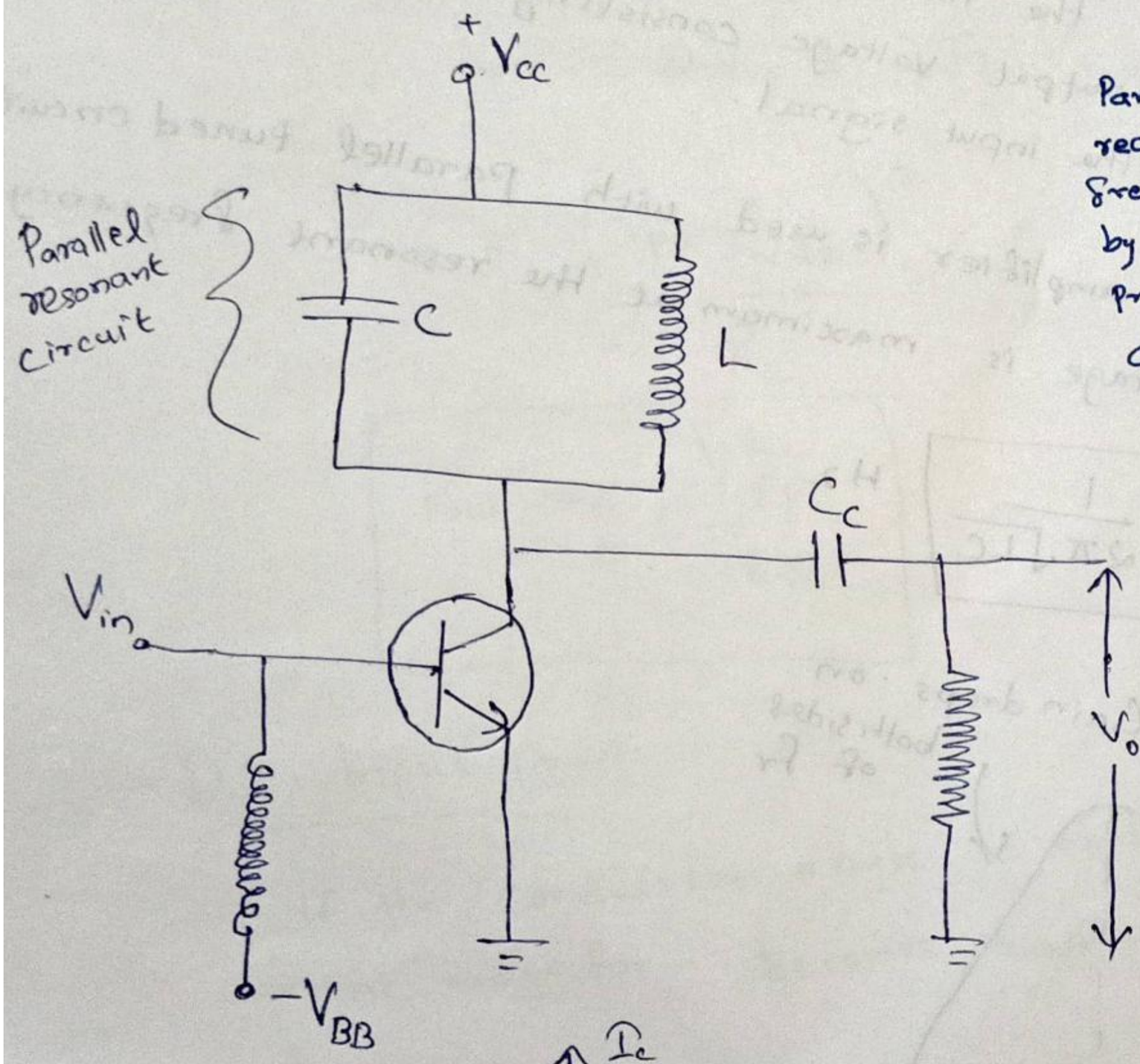
* But there will be a decrease in the output power due to the negative feedback effect

* The efficiency of class AB amplifier is greater than class A amplifier and slightly less than class B amplifier.

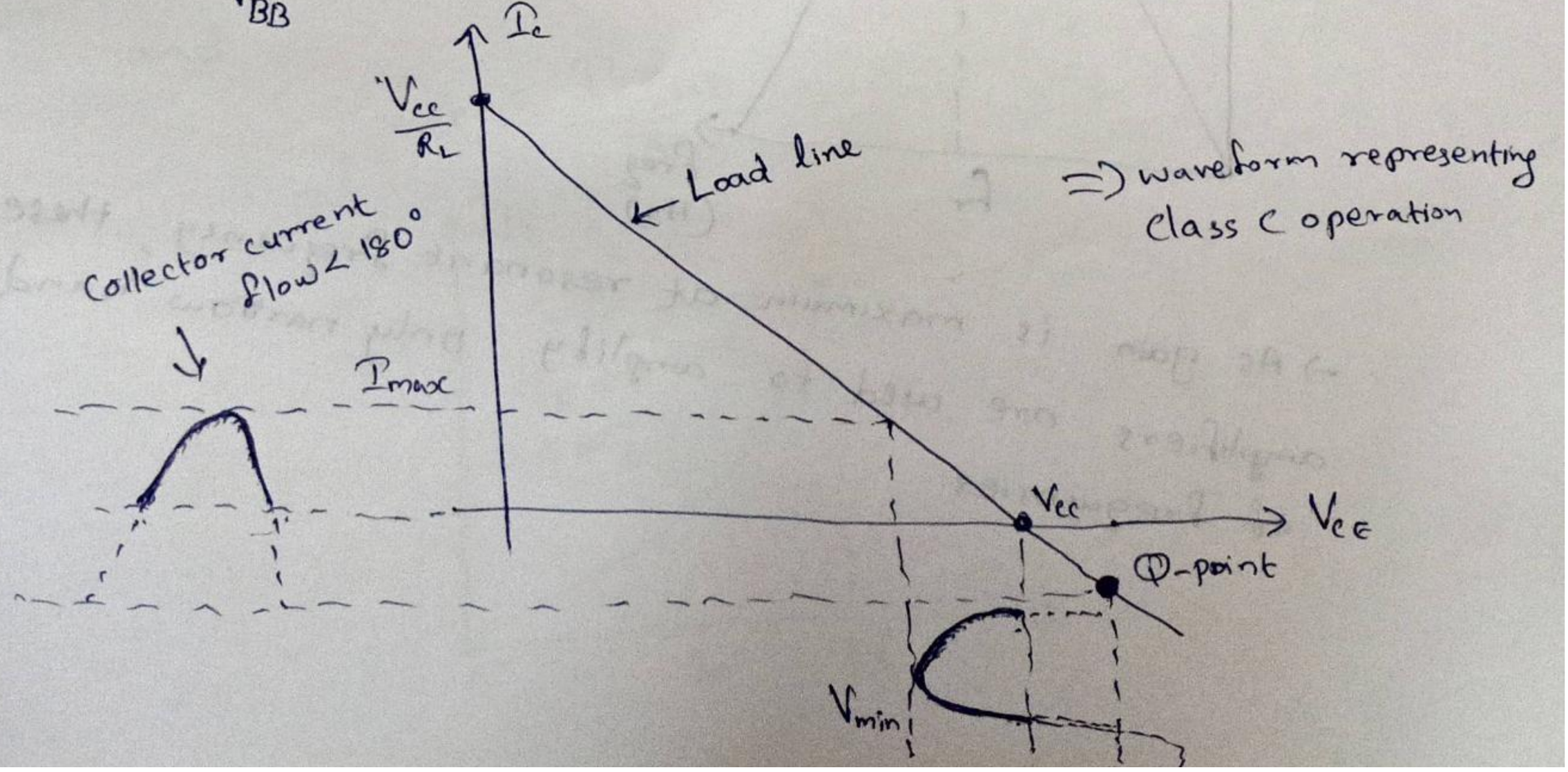
CLASS C Amplifier

* Power amplifier is said to be class C amplifier, if the Q-point and the input signal are selected. Such that the output signal is obtained for less than a half cycle for a full input cycle.

* For this operation, the Q-point is to be shifted below X-axis.



Parallel resonance circuit recover the fundamental frequency of i/p signal by filtering the harmonics present in the o/p signal of class C power amplifier



⇒ waveform representing class C operation

* A parallel resonant circuit acts as a load impedance.

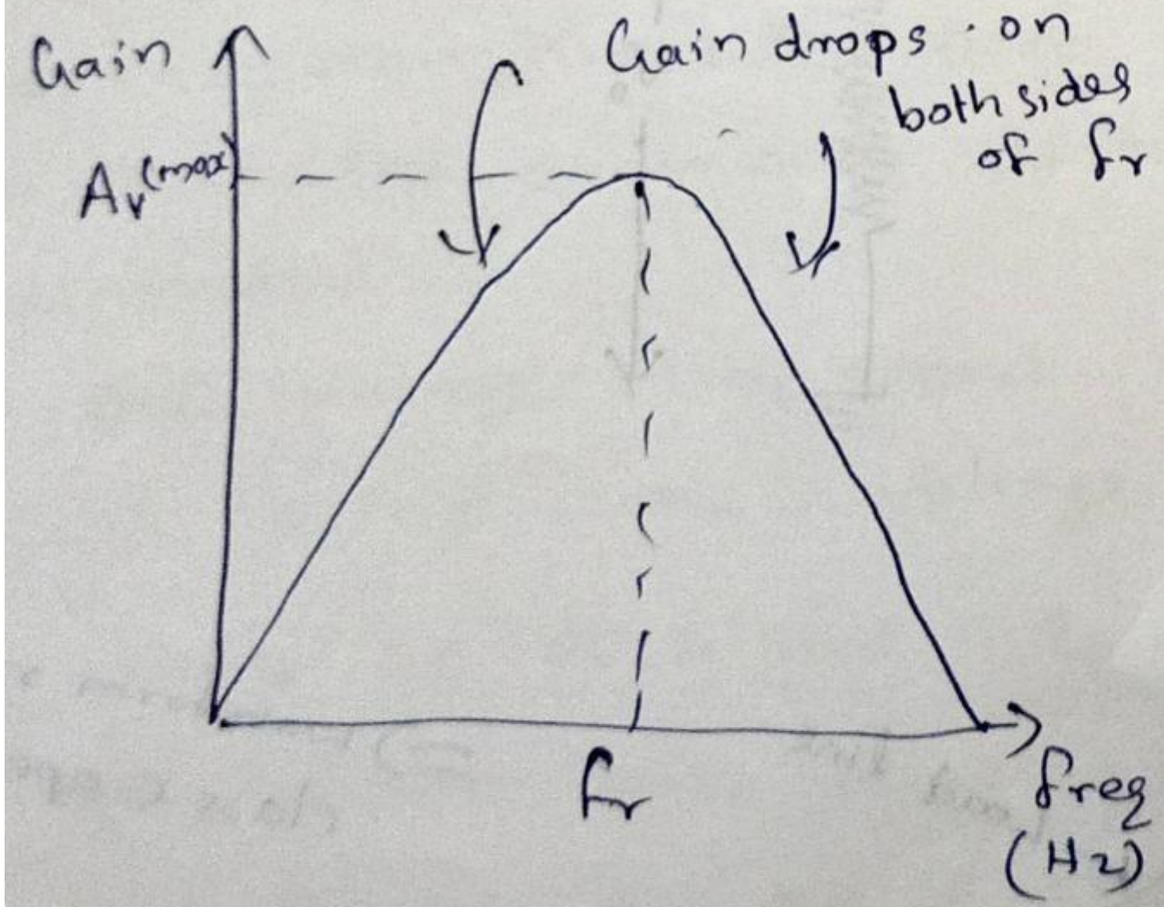
* The collector current flows for less than half cycle, hence it consist of a series of pulses with the harmonics of the input signal.

* A parallel tuned circuit acting as a load is tuned to the input frequency.

* Thus it filters the harmonic frequencies and produce a sine wave output voltage consisting of the fundamental component of the input signal.

* As Class C amplifier is used with parallel tuned circuit, the output voltage is maximum at the resonant frequency.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad Hz$$



→ As gain is maximum at resonant frequency, these amplifiers are used to amplify only narrow band of frequencies.

Output Power

* If the r.m.s value of output voltage across load resistance is measured then the output power is given by

$$P_{out} = \frac{V_{rms}^2}{R_L}$$

$$V_{PP} = 2V_m = 2\sqrt{2}\, V_{rms}$$

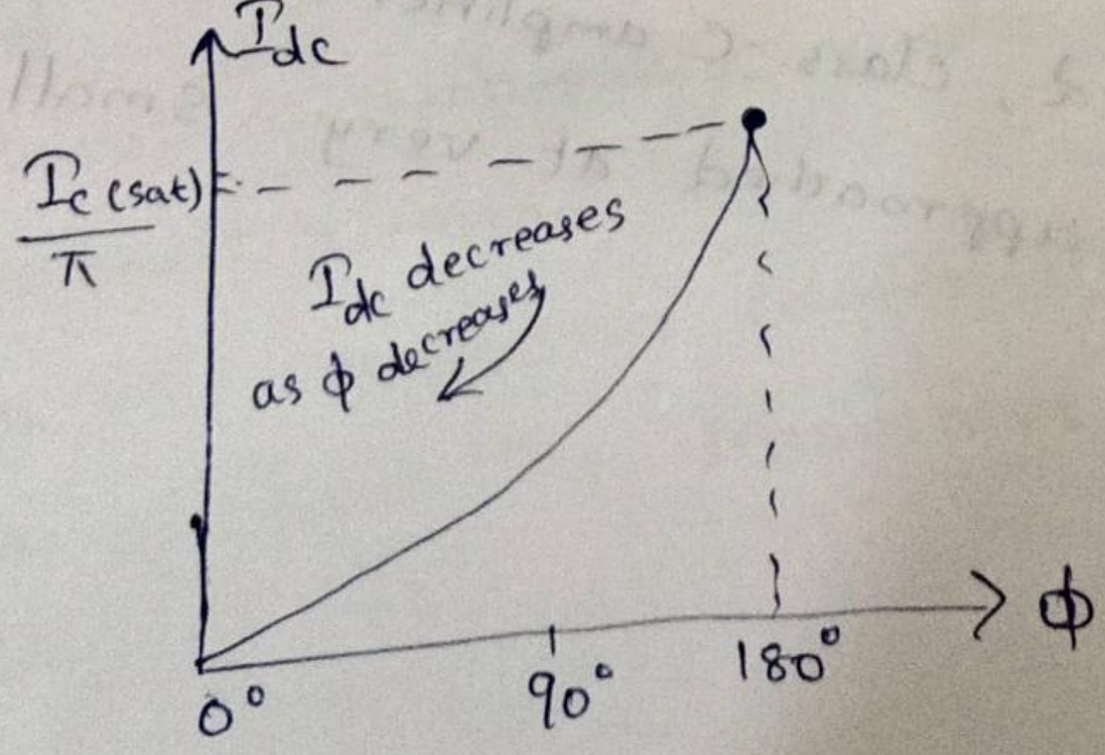
$$P_{out} = \frac{\left(V_{PP}/2\sqrt{2}\right)^2}{R_L}$$

$$\boxed{P_{out} = \frac{V_{PP}^2}{8R_L}}$$

D.C. Input Power

If the conduction angle is made 180°, then the current waveform becomes half wave rectified waveform and

$$I_{dc} = \frac{I_{c(sat)}}{\pi}$$

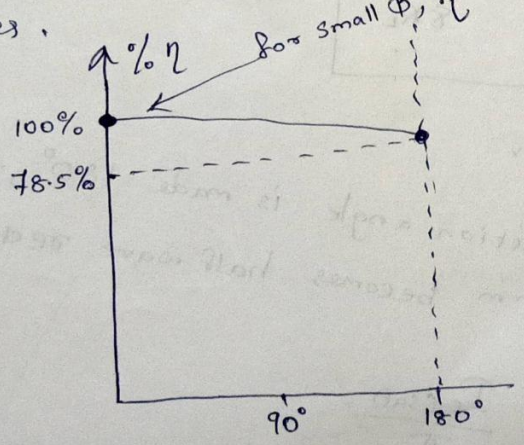


$$P_{DC} = V_{cc} I_{dc}$$

Efficiency

$$\%\eta = \frac{P_{out}}{P_{DC}} \times 100 = \frac{P_{out}}{V_{cc} I_{dc}} \times 100$$

* In the class C amplifier, most of the dc input power is converted into a.c load power because the transistor and coil losses are small.
* When the conduction angle is 180°, the efficiency is 78.5%.
* The efficiency increases when conduction angle decreases.



→ As indicated, class C amplifier has maximum efficiency of 100% approached at very small conduction angles.

VIDEO AMPLIFIERS

A transistor amplifier is limited in its frequency response. A VIDEO AMPLIFIER should have a frequency response of 10 hertz (10Hz) to 6 megahertz (6 MHz). The question has probably occurred to you: How is it possible to "extend" the range of frequency response of an amplifier?

HIGH-FREQUENCY COMPENSATION FOR VIDEO AMPLIFIERS

If the frequency-response range of an audio amplifier must be extended to 6 megahertz (6 MHz) for use as a video amplifier, some means must be found to overcome the limitations of the audio amplifier.The capacitance of an amplifier circuit and the inter-electrode capacitance of the transistor (or electronic tube) cause the higher frequency response to be limited. In some ways capacitance and inductance can be thought of as opposites. As stated before, as frequency increases, capacitive reactance decreases, and inductive reactance increases. Capacitance opposes changes in voltage, and inductance opposes changes in current. Capacitance causes current tolead voltage, and inductance causes voltage to lead current. Since frequency affects capacitive reactance and inductive reactance in opposite ways, and since it is the capacitive reactance that causes the problem with high-frequency response, inductors are added to an amplifier circuit to improve the high-frequency response. This is called *HIGH-FREQUENCYCOMPENSATION*.

Inductors (coils), when used for high-frequency compensation, are called PEAKINGCOILS. Peaking coils can be added to a circuit so they are in series with the output signal path or in parallel to the output signal path. Instead of only in series or parallel, a combination of peaking coils in series and parallel with the output signal path can also be used for high-frequency compensation. As in all electronic circuits, nothing comes free. The use of peaking coils WILL increase the frequency response of an amplifier circuit, but it will also lower the gain of the amplifier.

Series Peaking

The use of a peaking coil in series with the output signal path is known as SERIES PEAKING.Figure 2-6 shows a transistor amplifier circuit with a series peaking coil. In this figure, R1 is theinput-signal-developing resistor. R2 is used for bias and temperature stability of Q1. C1 is the by-pass capacitor for R2. R3 is the load resistor for Q1 and develops the output signal. C2 is the coupling capacitor which

couples the output signal to the next stage. "Phantom" capacitor C_{OUT} represents the output capacitance of the circuit, and "phantom" capacitor C_{IN} represents the input capacitance of the next stage.

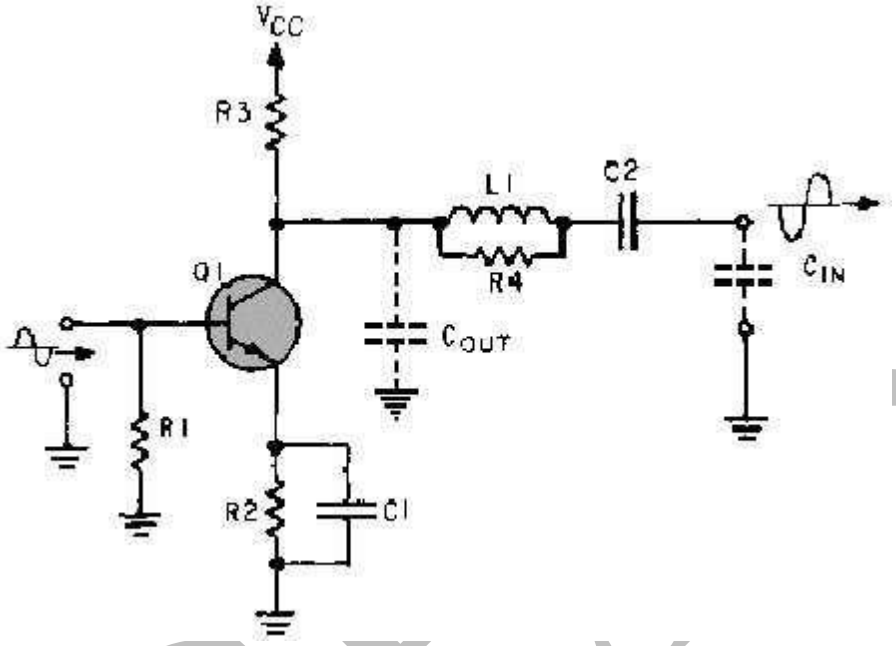


Figure 2-6.—Series peaking coil.

You know that the capacitive reactance of C_{OUT} and C_{IN} will limit the high-frequency response of the circuit. L1 is the series peaking coil. It is in series with the output- signal path and isolates C_{OUT} from C_{IN}.R4 is called a "swamping" resistor and is used to keep L1 from overcompensating at a narrow range of frequencies. In other words, R4 is used to keep the frequency-response curve flat. If R4 were not used with L1, there could be a "peak" in the frequency-response curve. (Remember, L1 is called a peaking coil.)

Shunt Peaking

If a coil is placed in parallel (shunt) with the output signal path, the technique is called SHUNTPEAKING. Figure 2-7 shows a circuit with a shunt peaking coil. With the exceptions of the "phantom" capacitor and the inductor, the components in this circuit are the same as those in figure 2-6. R1 is the input-signal-developing resistor. R2 is used for bias and temperature stability. C1 is the bypass capacitor for R2. R3 is the load resistor for Q1 and develops the output signal. C2 is the coupling capacitor which couples the output signal to the next stage.

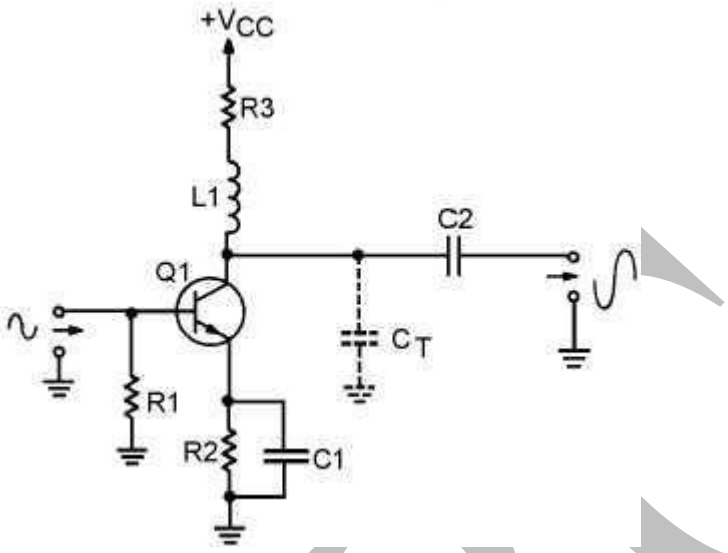


Figure 2-7.—Shunt peaking coil.

The "phantom" capacitor, C_T, represents the total capacitance of the circuit. Notice that it tends to couple the output signal to ground.L1 is the shunt peaking coil. While it is in series with the load resistor (R3), it is in parallel (shunt)with the output- signal path. Since inductive reactance increases as frequency increases, the reactance of L1 develops more output signal as the frequency increases. At the same time, the capacitive reactance of CT is decreasing as frequency increases. This tends to couple more of the output signal to ground. The increased inductive reactance counters the effect of the decreased capacitive reactance and this increases the high-frequency response of the amplifier.

Combination Peaking

You have seen how a series peaking coil isolates the output capacitance of an amplifier from the input capacitance of the next stage. You have also seen how a shunt peaking coil will counteract the effects of the total capacitance of an amplifier. If these two techniques are used together, the combination is more effective than the use of either one alone. The use of both series and shunt peaking coils is known as *COMBINATION PEAKING*. An amplifier circuit with combination peaking is shown in figure 2-8. In figure 2-8 the peaking coils are L1 and L2. L1 is a shunt peaking coil, and L2 is a series peaking coil.

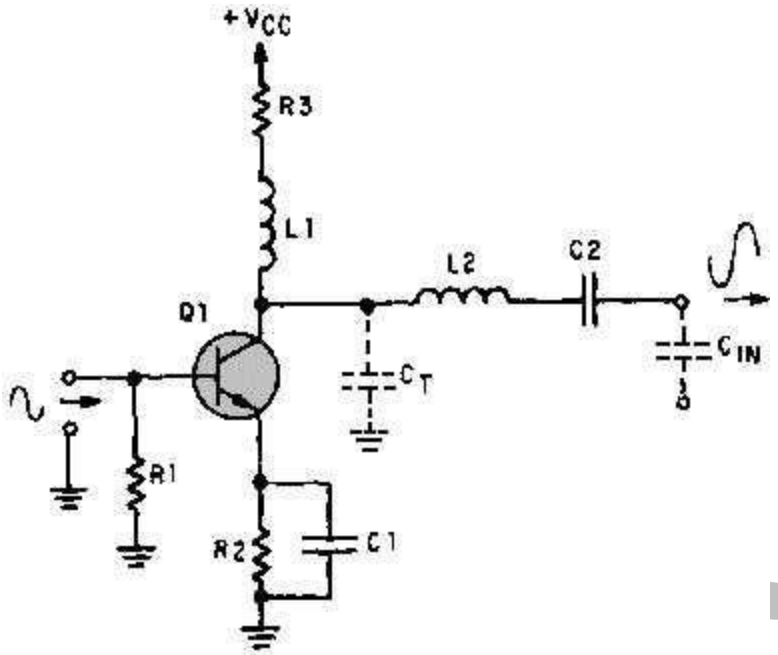


Figure 2-8.—Combination peaking.

The "phantom" capacitor C_T represents the total capacitance of the amplifier circuit. "Phantom" capacitor C_{IN} represents the input capacitance of the next stage. Combination peaking will easily allow an amplifier to have a high-frequency response of 6 megahertz (6 MHz).

LOW-FREQUENCY COMPENSATION FOR VIDEO AMPLIFIERS

Now that you have seen how the high-frequency response of an amplifier can be extended to 6megahertz (6 MHz), you should realize that it is only necessary to extend the low-frequency response to10 hertz (10 Hz) in order to have a video amplifier. Once again, the culprit in low-frequency response is capacitance (or capacitive reactance). But this time the problem is the coupling capacitor between the stages. At low frequencies the capacitive reactance of the coupling capacitor (C2 in figure 2-8) is high. This high reactance limits the amount of output signal that is coupled to the next stage. In addition, the RC network of the coupling capacitor and the signal-developing resistor of the next stage cause a phase shift in the output signal.

(*Refer to NEETS, Module 2, for a discussion of phase shifts in RC networks.) Both of* these problems (poor low-frequency response and phase shift) can be solved by adding a parallel RC network in series with the load resistor. This is shown in figure 2-9.

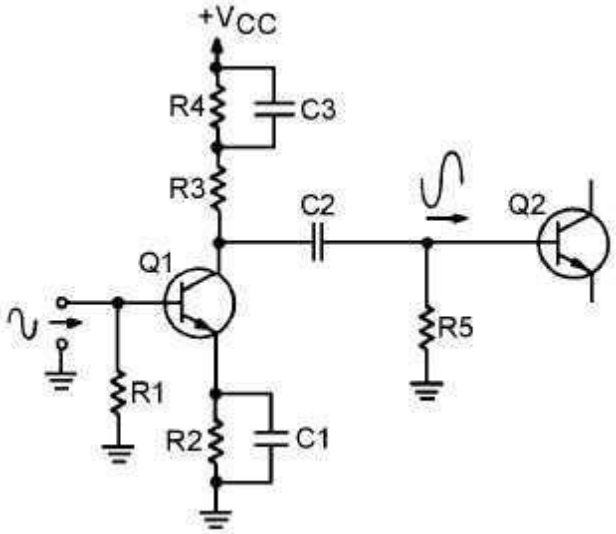


Figure 2-9.—Low frequency compensation network.

The complete circuitry for Q2 is not shown in this figure, as the main concern is the signal-developing resistor (R5) for Q2. The coupling capacitor (C2) and the resistor (R5) limit the low-frequency response of the amplifier and cause a phase shift. The amount of the phase shift will depend upon the amount of resistance and capacitance. The RC network of R4 and C3 compensates for the effects of C2 and R5 and extends the low-frequency response of the amplifier. At low frequencies, R4 adds to the load resistance (R3) and increases the gain of the amplifier. As frequency increases, the reactance of C3 decreases. C3 then provides a path around R4 and the gain of the transistor decreases. At the same time, the reactance of the coupling capacitor (C2) decreases and more signal is coupled to Q2.Because the circuit shown in figure 2-9 has no high-frequency compensation, it would not be a very practical video amplifier.

TYPICAL VIDEO-AMPLIFIER CIRCUIT

There are many different ways in which video amplifiers can be built. The particular configuration of a video amplifier depends upon the equipment in which the video amplifier is used. The circuit shown in figure 2-10 is only one of many possible video-amplifier circuits. Rather than reading about what each component does in this circuit, you can see how well you have learned about video amplifiers by answering

the following questions. You should have no problem identifying the purpose of the components because similar circuits have been explained to you earlier in the text.

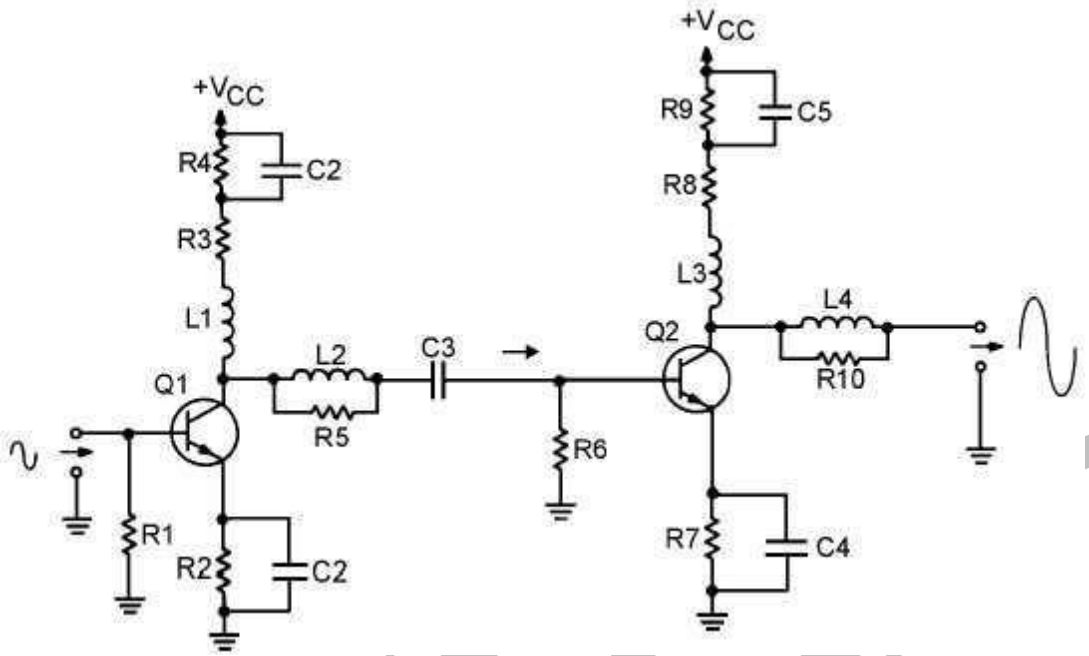


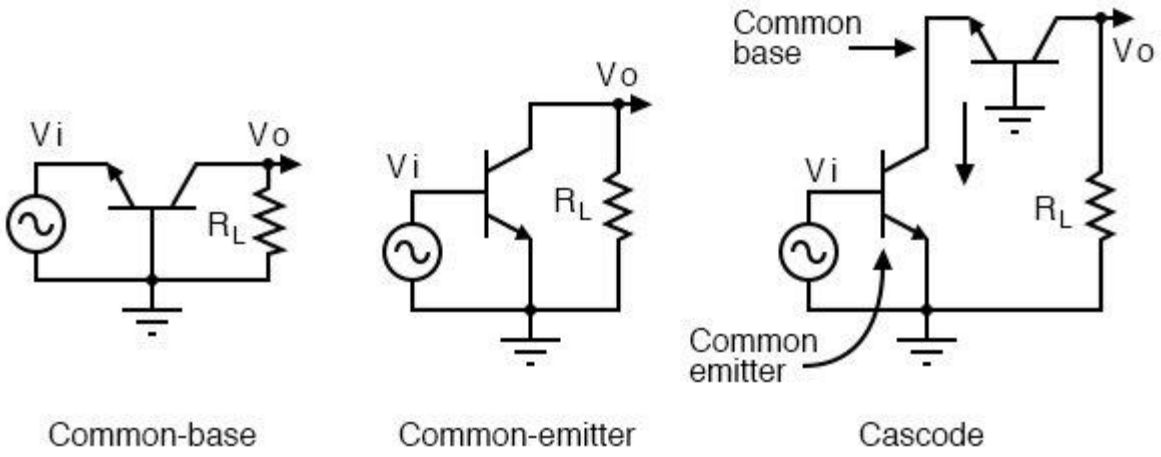
Figure 2-10.—Video amplifier circuit.

CASCODE AMPLIFER

While the C-B (common-base) amplifier is known for wider bandwidth than the C-E (common-emitter) configuration, the low input impedance (10s of Ω) of C-B is a limitation for many applications. The solution is to precede the C-B stage by a low gain C-E stage which has moderately high input impedance (kΩs).

The stages are in a *cascode* configuration stacked in series, as opposed to cascaded for a standard amplifier chain.

“Capacitor coupled three stage common-emitter amplifier” Capacitor coupled for a cascade example. The cascode amplifier configuration has both wide bandwidth and a moderately high input impedance.



Common-base Common-emitter Cascode

The cascode amplifier is combined common-emitter and common-base. This is an AC circuit equivalent with batteries and capacitors replaced by short circuits.

Bandwidth Capacitance and the Miller Effect

The key to understanding the wide bandwidth of the cascode configuration is the *Miller effect*. **The Miller effect is the multiplication of the bandwidth robbing collector-base capacitance by voltage gain Av.** This C-B capacitance is smaller than the E-B capacitance. Thus, one would think that the C-B capacitance would have little effect. However, in the C-E configuration, the collector output signal is out of phase with the input at the base. The collector signal capacitively coupled back opposes the base signal. Moreover, the collector feedback is (1-Av) times larger than the base signal. Keep in mind that Av is a negative number for the inverting C-E amplifier. Thus, the small C-B capacitance appears (1+|Av|) times larger than its actual value. This capacitive gain reducing feedback increases with frequency, reducing the high frequency response of a C-E amplifier.

MODULE 5

OSCILLATORS AND MULTIVIBRATORS

Oscillators

* Electronic oscillator circuits are generators of Periodic signal waveform without having any external input signal source.
* During the process of generation of AC signals, Oscillators draws DC power from supply source and converts it into AC power.

Classification of Oscillators

Output signal waveform

1) Sinusoidal Oscillators
2) Non-sinusoidal oscillator such as Relaxation oscillators
3) Multivibrators, Schmitt trigger, Saw tooth generators.

Frequency of output voltage

1) Fixed frequency oscillators
2) Variable frequency oscillators

Frequency band.

1) Audio frequency Oscillators 20Hz to 20 KHz
2) RF oscillators 30 KHz to 30 MHz
3) VHF oscillators 30 MHz to 300 MHz
4) UHF oscillators 300 MHz to 3 GHz
5) Microwave frequency oscillators above 3GHz.

Principles of generating oscillations

1) Oscillators using positive feedback
2) Negative resistance oscillators
3) Crystal controlled oscillators.

Frequency determining circuit components

1) RC Oscillators (Low-frequency oscillators)
2) LC oscillators (High frequency oscillators)

Name of the inventor of Oscillator circuits

1) Hartley Oscillator
2) Colpitts Oscillator

Barkhausen Criterion for Oscillations

(1) $|A\beta| = 1$

(2) $\angle A\beta = 360^\circ$ or 0°

when the loop gain $A\beta$ is made equal to unity.

$$A_f = \frac{A}{1-|A\beta|} = \frac{A}{1-1} = \frac{A}{0} = \infty$$

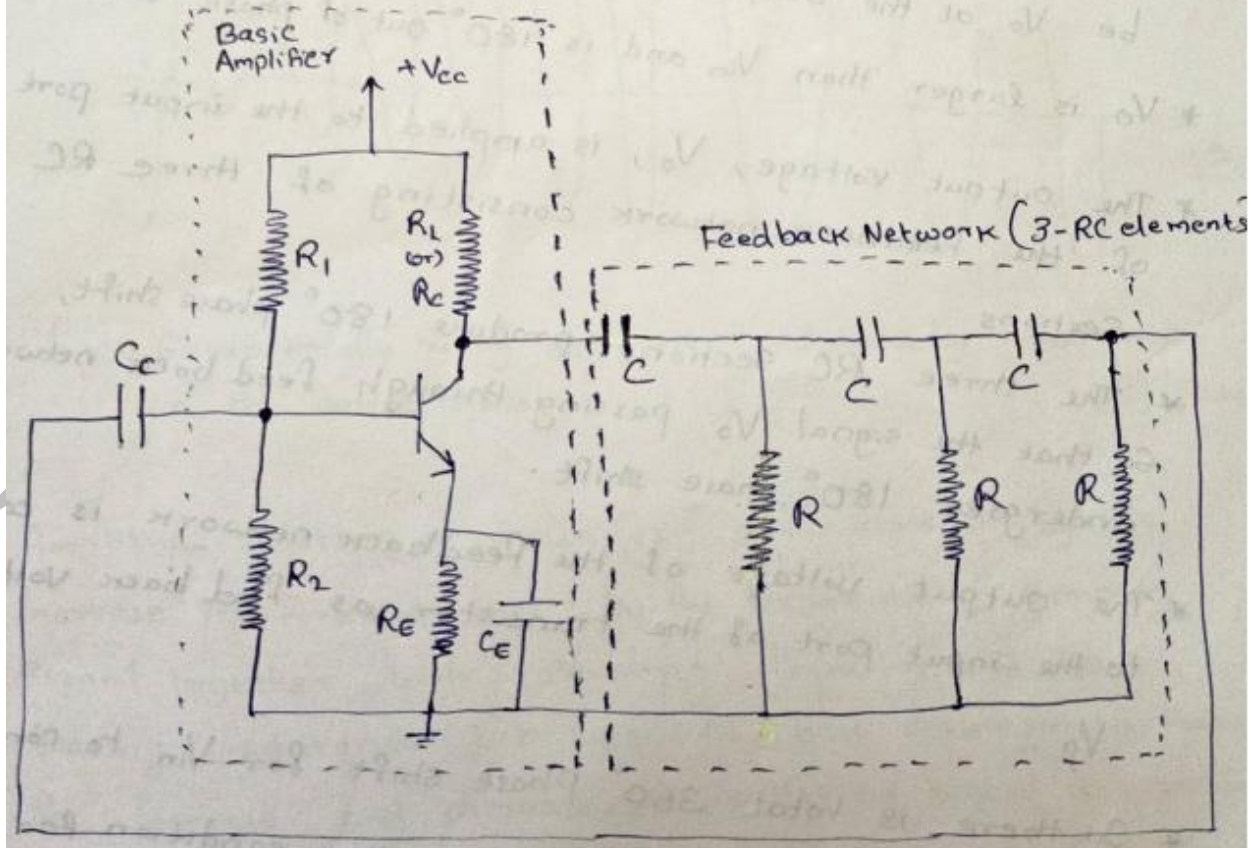
* Then the circuit oscillates.

* Infinite gain at the start of oscillations is controlled by non linearity of active device, so that the output signal of oscillator is stable.

In real systems no external input signal is applied to an oscillator. Only the condition $A\beta = 1 \angle 360^\circ$ or 0° must be satisfied to start and maintain the self-sustained oscillations

* Oscillator output signal undergoes a total phaseshift of 360° or 0°. The signal undergoes a phase shift of 180° in the internal amplifier and 180° phaseshift in 'feedback network'.

RC Phase Shift Oscillator



* When the DC Source is switched on, the random movement of charge carriers through the active device, the transistor and the circuit components produce a noise signal 'V_n' (white noise containing signal frequencies from 0 Hz to infinite Hz)

* Noise signal 'V_n' is of the order of a few Picovolts at the input port of the transistor.

* V_n acts as the Virtual input signal V_{in}.

* V_n is amplified with gain A. Let the amplified voltage be V_o at the output port of the transistor.

* V_o is larger than V_{in} and is 180° out of phase with V_{in}.

* The output voltage, V_o, is applied to the input port of the feedback network consisting of three RC sections

* The three RC sections produce 180° phase shift, So that the signal V_o passing through feed back network undergoes 180° phase shift.

* The output voltage of the feedback network is connect to the input port of the transistor as feed back voltage V_f.

So there is total 360° phase shift for V_{in} to come back as V_f and satisfies the condition for positive feedback

The two signals are in phase and their instantaneous amplitude get added.

* At this time the effective input signal V_{in} increases
* This cycle of events repeats and the output voltage goes on increasing unbounded till the setting in of the non-linearity of the active device that clamps the output voltage to a constant desired output voltage V_o.

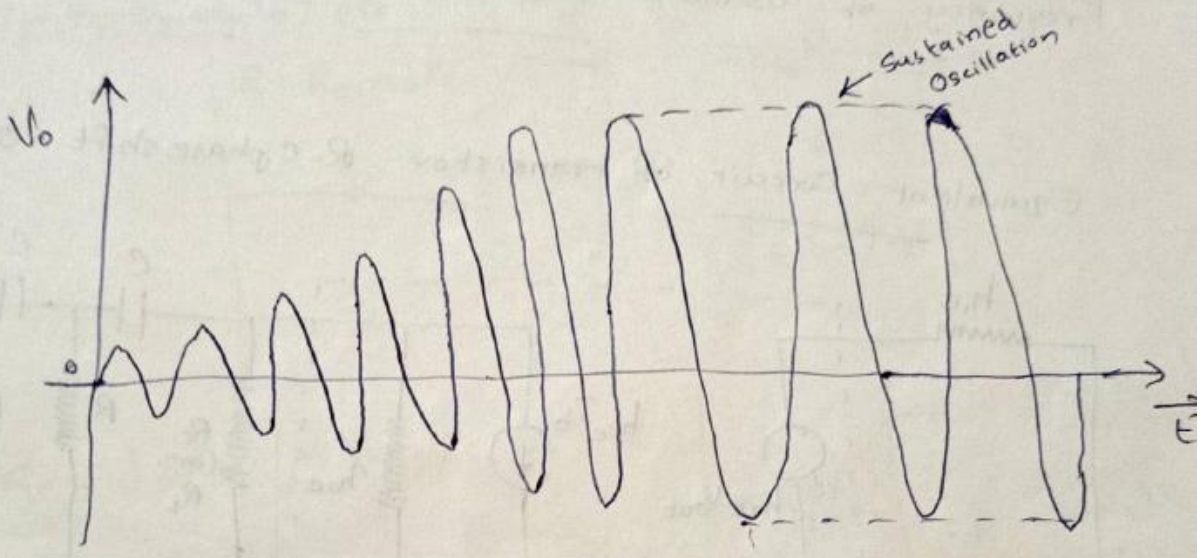


Fig:- Exponentially rising oscillations clamped by nonlinearity of the active device.

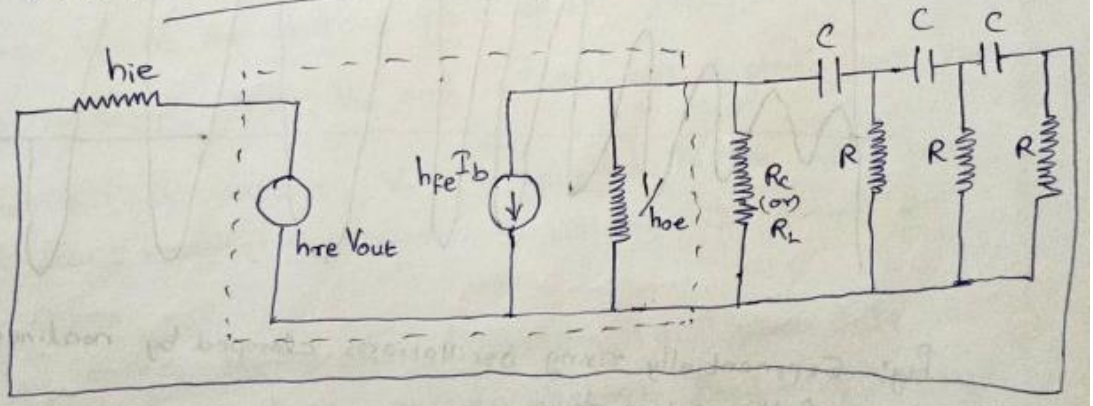
* The frequency of the output sine wave is decided the three RC sections in the feedback network and R_L according to the equation

$$f_o = \frac{1}{2\pi RC\sqrt{6+4\left(\frac{R_L}{R}\right)}} = \frac{1}{2\pi RC\sqrt{6+4K}} \text{ Hz}$$

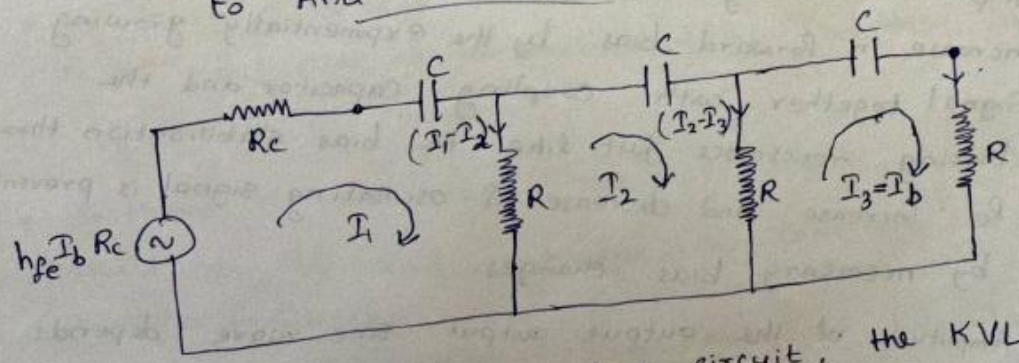
$$\left[\because K = R_L/R\right]$$

Frequency of oscillations of RC phase shift Oscillator

Equivalent Circuit of transistor R-C phase shift Oscillator



Modified equivalent Circuit of RC-phase shift oscillator to find the frequency of oscillation



* from this modified equivalent circuit, the KVL mesh equations are as follows!

Mesh equations

$$(R_c + R - jX_c) I_1 - R I_2 - h_{fe} R_c I_b = 0$$

$$-R I_1 + (2R - jX_c) I_2 - R I_b = 0$$

$$0 - R I_2 + (2R - jX_c) I_b = 0$$

As I_1, I_2, I_3 (or I_b) are non vanishing, determinant formed by coefficient $= 0$

$$\Delta \equiv \begin{vmatrix} R + R_c - jX_c & -R & -h_{fe} R_c \\ -R & 2R - jX_c & -R \\ 0 & -R & 2R - jX_c \end{vmatrix} = 0$$

$$\Delta = (R + R_c - jX_c) \begin{vmatrix} 2R - jX_c & -R \\ -R & 2R - jX_c \end{vmatrix} - (-R) \begin{vmatrix} -R & -h_{fe} R_c \\ -R & 2R - jX_c \end{vmatrix} = 0$$

$$= (R + R_c - jX_c) \left[(2R - jX_c)^2 - R^2 \right] + R \left[\left(-R(2R - jX_c) - h_{fe} R_c R \right) \right]$$

$$= (R + R_c - jX_c) \left(4R^2 - j4RX_c - X_c^2 - R^2 \right) + R \left(-2R^2 + jX_c R - h_{fe} R_c R \right) = 0$$

$$= 4R^3 - j4R^2 X_c - X_c^2 R - R^3 + 4R^2 R_c - j4RR_c X_c - X_c^2 R_c$$

$$- R^2 R_c - j4R^2 X_c - 4RX_c^2 + jX_c^3 + jR^2 X_c$$

$$- 2R^3 + jX_c R^2 - h_{fe} R_c R^2 = 0$$

$$R^3 + R^2 \cdot R_c(3-h_{fe}) - 5R \cdot X_c^2 - R_c X_c^2$$
$$- j(X_c^3 - 6R^2 X_c - 4 X_c R \cdot R_c) = 0$$

Imaginary part = 0

$$X_c^3 - X_c(6R^2 + 4R \cdot R_c) = 0$$

$$X_c^2 = 6R^2 + 4RR_c$$

$$\frac{1}{\omega^2 C^2} = 6R^2 + 4R \cdot R_c$$

$$\omega^2 C^2 = \frac{1}{6R^2 + 4R \cdot R_c} \Rightarrow \omega^2 = \frac{1}{C^2(6R^2 + 4R \cdot R_c)}$$

$$\omega = \frac{1}{\sqrt{C^2(6R^2 + 4R \cdot R_c}} = \frac{1}{RC\sqrt{6 + 4\frac{R_c}{R}}}$$

$$2\pi f = \frac{1}{RC\sqrt{6 + 4\frac{R_c}{R}}} \quad \left[\because \frac{R_c}{R} = K\right)$$

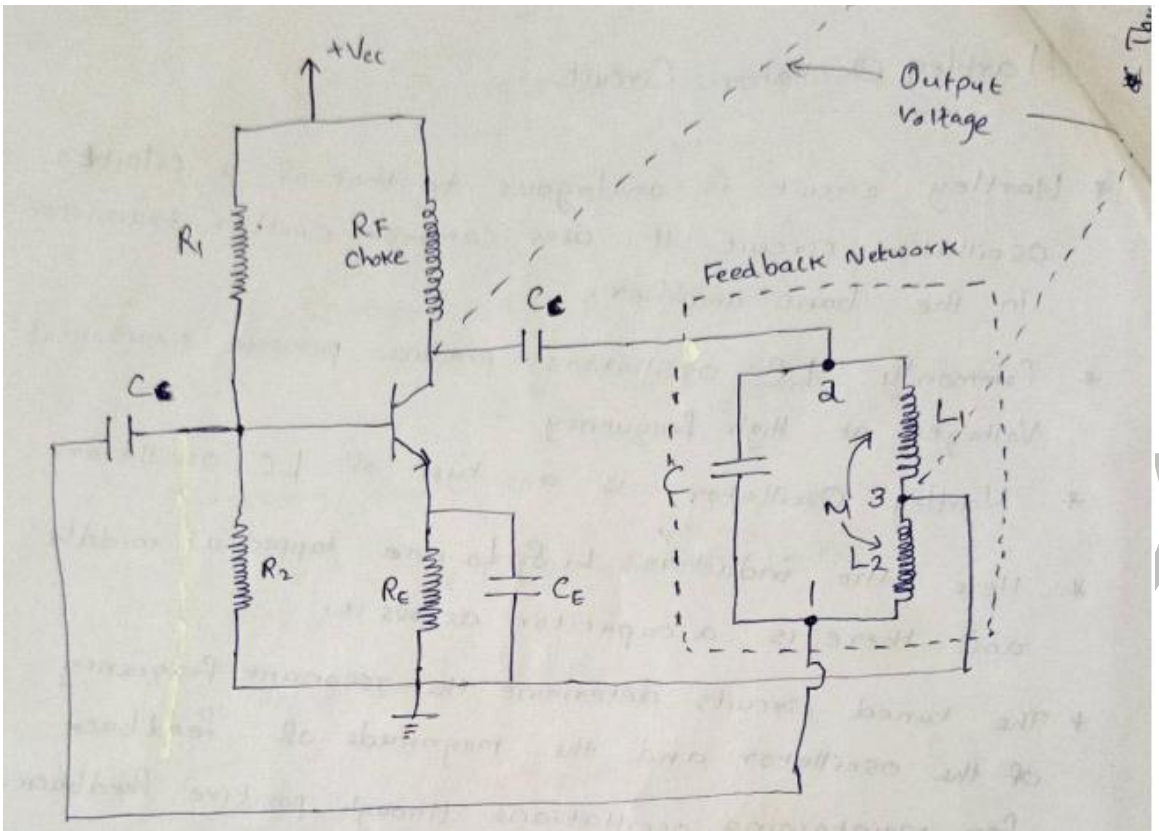
$$f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

RC phase shift oscillators are capable of generating frequencies of a few Hz to several KHz and are particularly suitable for audio frequency oscillators.

By varying the elements of three RC networks, variable frequency operation can be achieved

Hartley Oscillator Circuit

* Hartley circuit is analogous to that of a colpitts oscillator circuit. It uses common Emitter transistor in the basic amplifier.
* Commonly LC oscillators produce periodic sinusoidal voltages at High frequency.
* Hartley Oscillator is a type of LC oscillator.
* Here the inductors L_1 & L_2 are tapped at middle and there is a capacitor across it.
* The tuned circuits determine the resonant frequency of the oscillator and the magnitude of feedback for maintaining oscillations through positive feedback.
* Radio frequency coil (RFC) (ωL) at the collector terminal act as a DC short and has a high impedance for high frequency oscillations ~~and has a high impedance for high frequency oscillations~~ and so high frequency signals are blocked from reaching the power supply.
* The supply voltage V_{cc}, parallel combination of R_E and C_E and potential divider R_1 and R_2 provide the necessary stabilised bias to the transistor.
* The phase shift network consists of the two inductors L_1 and L_2.



- When the circuit is switched on, transient current is produced in the tank circuit and damped oscillations are set up in the tuned circuit.

Refering to the Hartley oscillator circuit, at any instant the voltages with respect to terminal 3 which is at ground, terminal 1 is positive and terminal 2 is negative and vice versa thus containing a phase shift of 180° with the common Emitter Transistor Amplifier.

The output voltage is across the inductor L_2.

- The coil L_2 is inductively coupled to coil L_1.
- Thus the induced voltage across L_1 forms the feed back voltage 'V_f', through C_c to the base of transistor

* Common Emitter operation of the transistor results in a phase shift of 180° and another 180° phase shift among the voltage across L_1 & L_2. The total phase shift around the loop is 360° or 0° and satisfies the Bharkhausen conditions (criteria) of oscillations

$$X_{L_1} = j\omega(L_1 + M)$$

$$X_{L_2} = j\omega(L_2 + M)$$

$$X_C = \frac{-j}{\omega C}$$

$$X_{L_1} + X_{L_2} + X_C = 0 \quad \text{(In a tuned circuit the total reactance = 0)}$$

$$\therefore \omega(L_1 + L_2 + 2M) = \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{C(L_1 + L_2 + 2M)} = \frac{1}{C L_{equ}}$$

$$\left[\because L_{equ} = L_1 + L_2 + 2M\right]$$

$$\therefore \boxed{f_0 = \frac{1}{2\pi\sqrt{C \cdot L_{equ}}}}$$

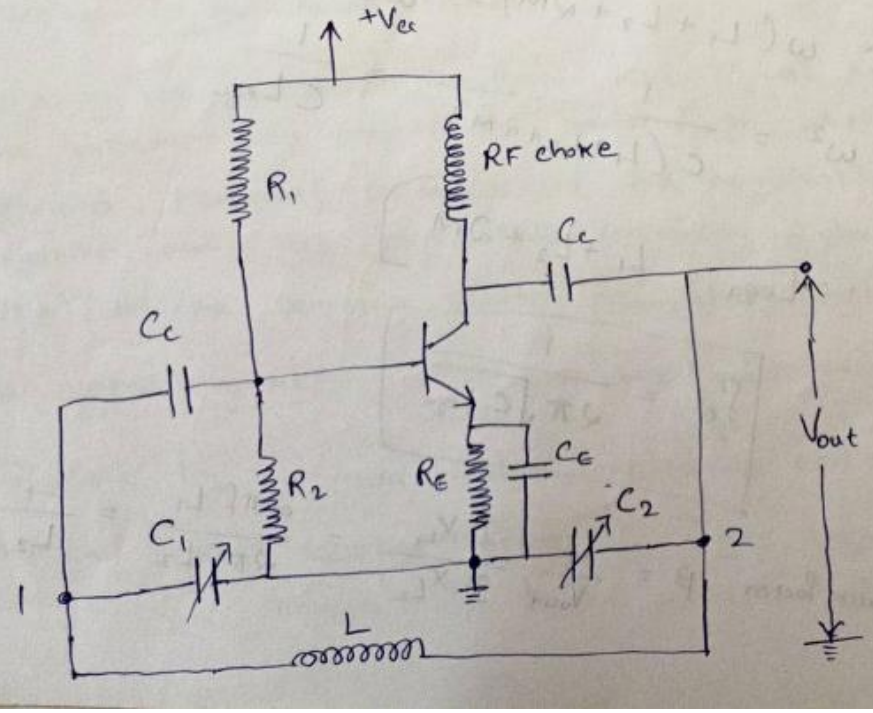
Feedback factor $\beta = \frac{V_f}{V_{out}} = \frac{I \cdot X_{L_1}}{I \cdot X_{L_2}} = \frac{2\pi f L_1}{2\pi f L_2} = \frac{L_1}{L_2}$

$A\beta = 1$ [from Barkhausen criteria]

$$A = \frac{1}{\beta} = \frac{L_2}{L_1}$$

* Hartley oscillator is used as RF oscillator.
* Frequency of oscillation can be changed by making the core movable (Varying the inductance) or by varying capacitance.
* It is used in Super heterodyne receiver.
* Disadvantage of Hartley Oscillator is that it cannot be used as low frequency oscillator since the value of inductors becomes large and size of inductors becomes bulky.

COLPITTS OSCILLATOR



* Radio frequency coil (RFC) (ωL - Inductive reactance) acts like

1) DC short to connect the DC supply voltage V_{cc} to the collector terminal of BJT &

2) Large impedance for AC signals that prevents high frequency output oscillations to reach power supply.

* DC supply V_{cc} in association with R_1, R_2 (voltage divider) and parallel combination of R_E & C_E at emitter terminal provide the necessary stabilised biasing voltages to the BJT.

* Common Emitter Amplifier introduces a phaseshift of 180° to the inherently generated noise signal due to the randomly moving charge carriers through the device.

* Another 180° phase shift is provided by the capacitive feed back for introducing positive feedback for oscillator action during the signal passage through the feedback circuit.

* The overall phase shift is 360° or 0° to the signals for satisfying the Bhark hausen condition to start and maintain the oscillations. and satisfy [$A\beta = 1$].

Oscillator Action & Frequency Selection

* The feedback network has two variable capacitors C_1 & C_2 in series whose centre is grounded and are shunted by an inductor L.

* The capacitor and inductor constitute a resonant circuit in the feedback loop to determine the frequency of oscillations of the circuit.

* The voltage across the capacitor C_2 is the oscillator's output voltage V_{out}.

* The voltage across the capacitor C_1 is the feedback voltage (V_f) to the input port of the active device (BJT) in the circuit.

* The tuned circuit with the inductor L and variation of the two capacitances C_1 & C_2 using ganged tuning for simultaneous variation set the condition for oscillations and Oscillator frequency.

$$X_{C_1} = \frac{-j}{\omega \cdot C_1}$$

$$X_{C_2} = \frac{-j}{\omega C_2}$$

$$X_L = j\omega L$$

$$X_{C_1} + X_{C_2} + X_{L_0} = 0$$

$$-\frac{j}{\omega C_1} - \frac{j}{\omega \cdot C_2} + j \cdot \omega \cdot L = 0$$

$$\omega \cdot L = \frac{1}{\omega \cdot C_1} + \frac{1}{\omega \cdot C_2}$$

$$\omega \cdot L = \frac{1}{\omega}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$$

$$\omega^2 = \frac{1}{L}\left[\frac{C_1 + C_2}{C_1 C_2}\right]$$

$$\omega^2 = \frac{1}{L} \cdot \frac{1}{C_{equ}} \qquad \left[\because C_{equ} = \frac{C_1 \cdot C_2}{C_1 + C_2}\right]$$

$$\omega = \frac{1}{\sqrt{L \cdot C_{eq}}}$$

$$\boxed{f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{equ}}}}$$

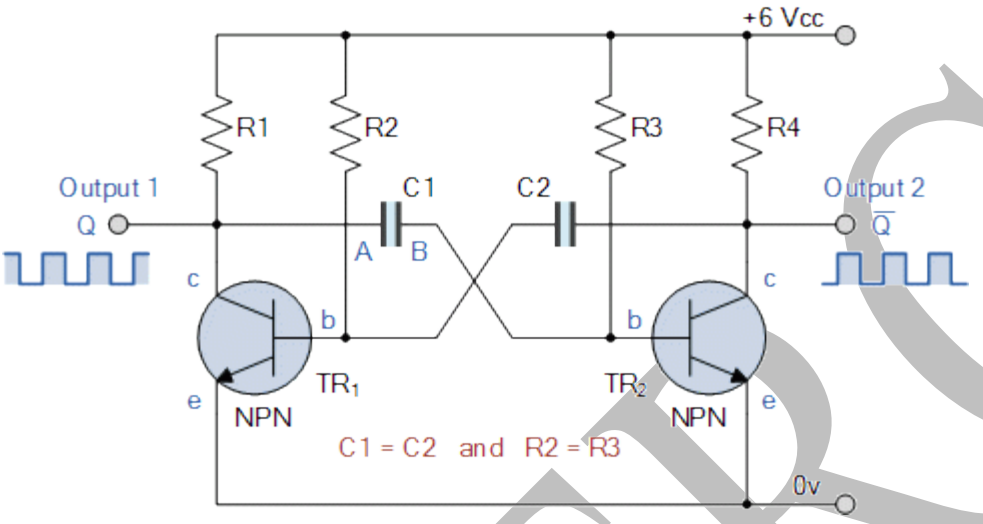
Feed back factor, $\beta = \frac{V_f}{V_{out}} = \frac{I \cdot X_{C_1}}{I \cdot X_{C_2}} = \frac{C_2}{C_1}$

From the condition $A\beta = 1$,

Gain $A = \frac{1}{\beta} = \frac{C_2}{C_1}$

Astable Multivibrator

Astable Multivibrators are free running oscillators which oscillate between two states continually producing two square wave output waveforms



Regenerative switching circuits such as **Astable Multivibrators** are the most commonly used type of relaxation oscillator because not only are they simple, reliable and ease of construction they also produce a constant square wave output waveform.

Unlike the Monostable Multivibrator or the Bistable Multivibrator we looked at in the previous tutorials that require an "external" trigger pulse for their operation, the **Astable Multivibrator** has automatic built in triggering which switches it continuously between its two unstable states both set and reset.

The **Astable Multivibrator** is another type of cross-coupled transistor switching circuit that has **NO** stable output states as it changes from one state to the other all the time. The astable circuit consists of two switching transistors, a cross-coupled feedback network, and two time delay capacitors which allows oscillation between the two states with no external triggering to produce the change in state.

In electronic circuits, astable multivibrators are also known as **Free-running Multivibrator** as they do not require any additional inputs or external assistance to oscillate. Astable oscillators produce a continuous square wave from its output or outputs, (two outputs no inputs) which can then be used to flash lights or produce a sound in a loudspeaker.

The basic transistor circuit for an **Astable Multivibrator** produces a square wave output from a pair of grounded emitter cross-coupled transistors. Both transistors either NPN or PNP, in the multivibrator are biased for linear operation and are operated as Common Emitter Amplifiers with 100% positive feedback.

This configuration satisfies the condition for oscillation when: ($\beta A = 1\angle 0^o$). This results in one stage conducting "fully-ON" (Saturation) while the other is switched "fully-OFF" (cut-off) giving a very high level of mutual amplification between the two transistors. Conduction is transferred from one stage to the other by the discharging action of a capacitor through a resistor

Assume a 6 volt supply and that transistor, TR_1 has just switched "OFF" (cut-off) and its collector voltage is rising towards Vcc, meanwhile transistor TR_2 has just turned "ON". Plate "A" of capacitor C1 is also rising towards the +6 volts supply rail of Vcc as it is connected to the collector of TR_1 which is now cut-off. Since TR_1 is in cut-off, it conducts no current so there is no volt drop across load resistor R_1.

The other side of capacitor, C1, plate "B", is connected to the base terminal of transistor TR_2 and at 0.6v because transistor TR_2 is conducting (saturation). Therefore, capacitor C1 has a potential difference of +5.4 volts across its plates, (6.0 – 0.6v) from point A to point B.

Since TR_2 is fully-on, capacitor C_2 starts to charge up through resistor R_2 towards Vcc. When the voltage across capacitor C_2 rises to more than 0.6v, it biases transistor TR_1 into conduction and into saturation.

The instant that transistor, TR_1 switches "ON", plate "A" of the capacitor which was originally at Vcc potential, immediately falls to 0.6 volts. This rapid fall of voltage on plate "A" causes an equal and instantaneous fall in voltage on plate "B" therefore plate "B" of C1 is pulled down to -5.4v (a reverse charge) and this negative voltage swing is applied the base of TR_2 turning it hard "OFF". One unstable state.

Transistor TR_2 is driven into cut-off so capacitor C1 now begins to charge in the opposite direction via resistor R3 which is also connected to the +6 volts supply rail, Vcc. Thus the base of transistor TR_2 is now moving upwards in a positive direction towards Vcc with a time constant equal to the C1 x R3 combination.

However, it never reaches the value of Vcc because as soon as it gets to 0.6 volts positive, transistor TR_2 turns fully "ON" into saturation. This action starts the whole process over again but now with capacitor C2 taking the base of transistor TR_1 to -5.4v while charging up via resistor R2 and entering the second unstable state.

Then we can see that the circuit alternates between one unstable state in which transistor TR_1 is "OFF" and transistor TR_2 is "ON", and a second unstable in which TR_1 is "ON" and TR_2 is "OFF" at a rate determined by the RC values. This process will repeat itself over and over again as long as the supply voltage is present.

The amplitude of the output waveform is approximately the same as the supply voltage, Vcc with the time period of each switching state determined by the time constant of the RC networks connected across the base terminals of the transistors. As the transistors are switching both "ON"

and “OFF”, the output at either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors. This could be corrected by using more components as we will discuss later.

If the two time constants produced by C2 x R2 and C1 x R3 in the base circuits are the same, the mark-to-space ratio (t1/t2) will be equal to one-to-one making the output waveform symmetrical in shape. By varying the capacitors, C1, C2 or the resistors, R2, R3 the mark-to-space ratio and therefore the frequency can be altered.

We saw in the RC Discharging tutorial that the time taken for the voltage across a capacitor to fall to half the supply voltage, 0.5Vcc is equal to 0.69 time constants of the capacitor and resistor combination. Then taking one side of the astable multivibrator, the length of time that transistor TR_2 is “OFF” will be equal to 0.69T or 0.69 times the time constant of C1 x R3. Likewise, the length of time that transistor TR_1 is “OFF” will be equal to 0.69T or 0.69 times the time constant of C2 x R2 and this is defined as.

Astable Multivibrators Periodic Time

$$\text{Periodic Time, } T = t_1 + t_2$$
$$t_1 = 0.69 C_1 R_3$$
$$t_2 = 0.69 C_2 R_2$$

Where, R is in Ω’s and C in Farads.

By altering the time constant of just one RC network the mark-to-space ratio and frequency of the output waveform can be changed but normally by changing both RC time constants together at the same time, the output frequency will be altered keeping the mark-to-space ratios the same at one-to-one.

If the value of the capacitor C1 equals the value of the capacitor, C2, C1 = C2 and also the value of the base resistor R2 equals the value of the base resistor, R3, R2 = R3 then the total length of time of the **Multivibrators** cycle is given below for a symmetrical output waveform.

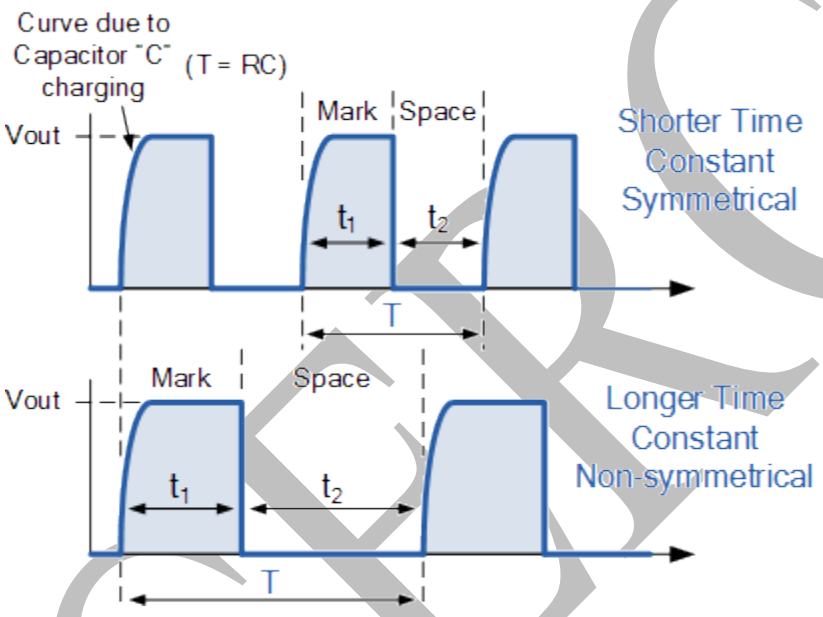
Frequency of Oscillation

$$f = \frac{1}{T} = \frac{1}{1.38RC}$$

Where, R is in Ω's, C is in Farads, T is in seconds and *f* is in Hertz.

and this is known as the "Pulse Repetition Frequency". So **Astable Multivibrators** can produce TWO very short square wave output waveforms from each transistor or a much longer rectangular shaped output either symmetrical or non-symmetrical depending upon the time constant of the RC network as shown below.

Astable Multivibrator Waveforms



Bistable Multivibrator

Bistable Multivibrators operate in a similar fashion to flip-flops producing one of two stable outputs which are the complement of each other

The **Bistable Multivibrator** is another type of two state device similar to the Monostable Multivibrator we looked at in the previous tutorial but the difference this time is that BOTH states are stable.

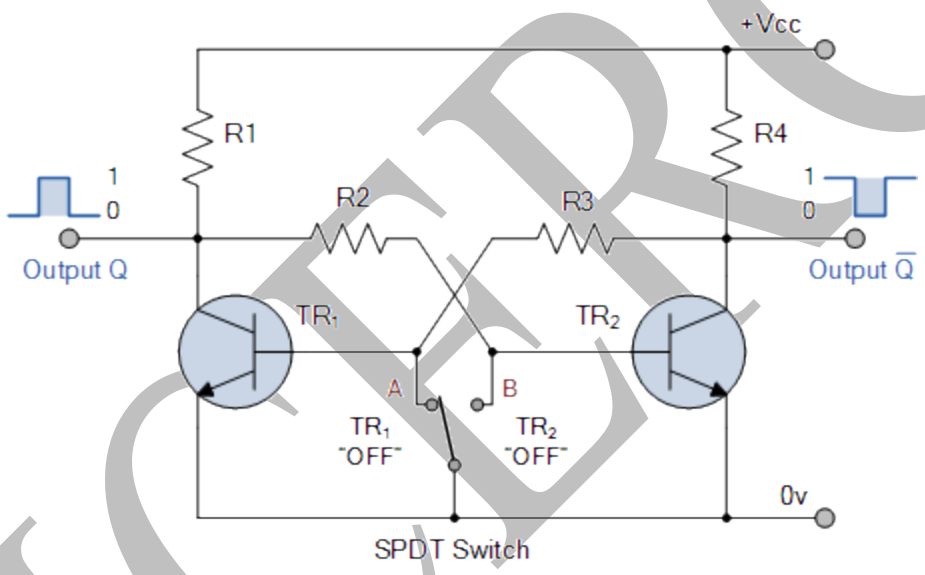
Bistable Multivibrators have **TWO** stable states (hence the name: "Bi" meaning two) and maintain a given output state indefinitely unless an external trigger is applied forcing it to change state.

The bistable multivibrator can be switched over from one stable state to the other by the application of an external trigger pulse thus, it requires two external trigger pulses before it returns back to its original state. As bistable multivibrators have two stable states they are more commonly known as Latches and Flip-flops for use in sequential type circuits.

The discrete **Bistable Multivibrator** is a two state non-regenerative device constructed from two cross-coupled transistors operating as "ON-OFF" transistor switches. In each of the two states, one of the transistors is cut-off while the other transistor is in saturation, this means that the bistable circuit is capable of remaining indefinitely in either stable state.

To change the bistable over from one state to the other, the bistable circuit requires a suitable trigger pulse and to go through a full cycle, two triggering pulses, one for each stage are required. Its more common name or term of "flip-flop" relates to the actual operation of the device, as it "flips" into one logic state, remains there and then changes or "flops" back into its first original state. Consider the circuit below.

Bistable Multivibrator Circuit



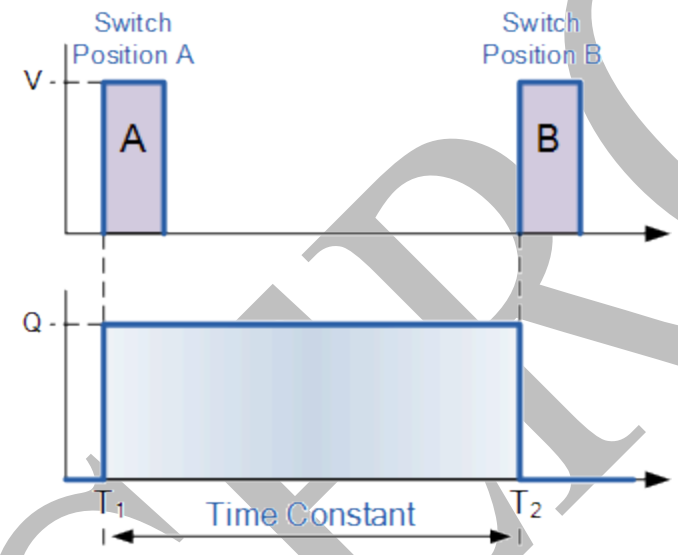
The **Bistable Multivibrator** circuit above is stable in both states, either with one transistor "OFF" and the other "ON" or with the first transistor "ON" and the second "OFF". Lets suppose that the switch is in the left position, position "A". The base of transistor TR_1 will be grounded and in its cut-off region producing an output at Q. That would mean that transistor TR_2 is "ON" as its base is connected to Vcc through the series combination of resistors R1 and R2. As transistor TR_2 is "ON" there will be zero output at Q, the opposite or inverse of Q.

If the switch is now move to the right, position "B", transistor TR_2 will switch "OFF" and transistor TR_1 will switch "ON" through the combination of resistors R3 and R4 resulting in an output at Q and zero output at Q the reverse of above. Then we can say that one stable state exists when transistor TR_1 is "ON" and TR_2 is "OFF", switch position "A", and another stable state exists when transistor TR_1 is "OFF" and TR_2 is "ON", switch position "B".

Then unlike the monostable multivibrator whose output is dependent upon the RC time constant of the feedback components used, the bistable multivibrators output is dependent upon the application of two individual trigger pulses, switch position “A” or position “B”.

So **Bistable Multivibrators** can produce a very short output pulse or a much longer rectangular shaped output whose leading edge rises in time with the externally applied trigger pulse and whose trailing edge is dependent upon a second trigger pulse as shown below.

Bistable Multivibrator Waveform



Manually switching between the two stable states may produce a bistable multivibrator circuit but is not very practical.

Monostable Multivibrator

Multivibrators are Sequential regenerative circuits either synchronous or asynchronous and are used extensively in electronic timing applications

Multivibrators produce an output wave shape resembling that of a symmetrical or asymmetrical square wave and as such are the most commonly used of all the square wave generators. Multivibrators belong to a family of oscillators commonly called “**Relaxation Oscillators**“.

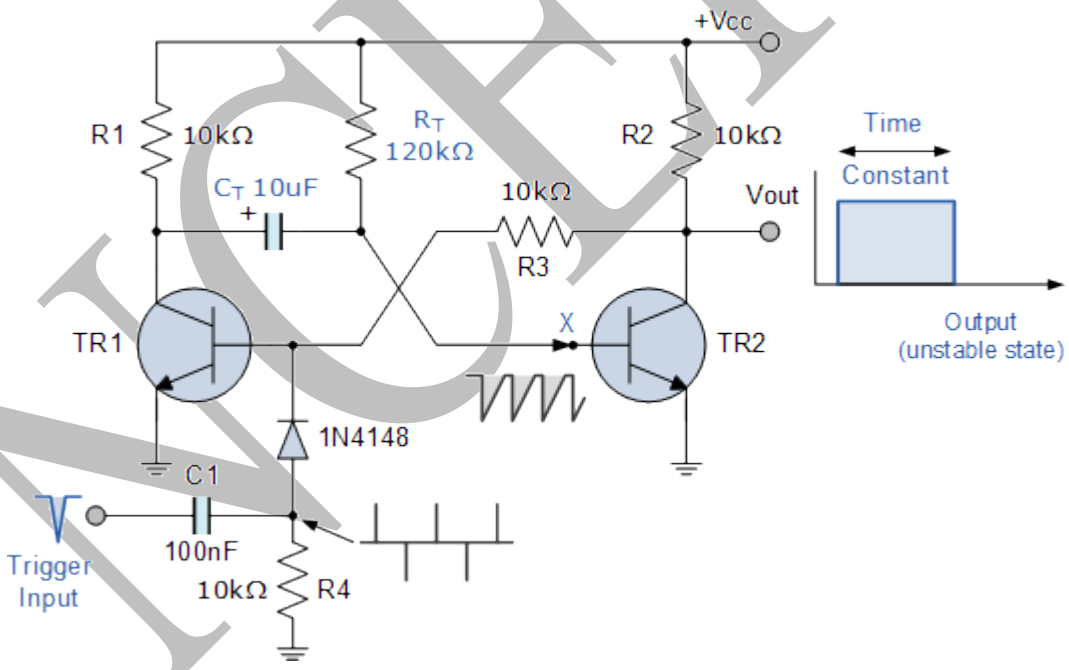
Generally speaking, discrete multivibrators consist of a two transistor cross coupled switching circuit designed so that one or more of its outputs are fed back as an input to the other transistor

with a resistor and capacitor (RC) network connected across them to produce the feedback tank circuit.

Multivibrators have two different electrical states, an output "HIGH" state and an output "LOW" state giving them either a stable or quasi-stable state depending upon the type of multivibrator. One such type of a two state pulse generator configuration are called **Monostable Multivibrators**.

Monostable Multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state.

The timing cycle of the monostable is determined by the time constant of the timing capacitor, C_T and the resistor, R_T until it resets or returns itself back to its original (stable) state. The monostable multivibrator will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.



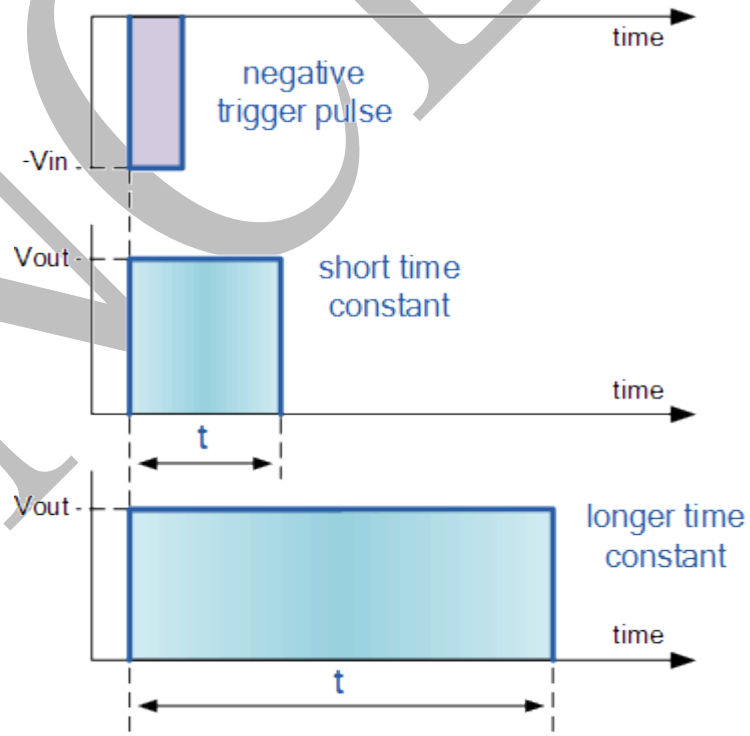
The basic collector-coupled transistor **Monostable Multivibrator** circuit and its associated waveforms are shown above. When power is firstly applied, the base of transistor TR2 is connected to Vcc via the biasing resistor, R_T thereby turning the transistor "fully-ON" and into saturation and at the same time turning TR1 "OFF" in the process. This then represents the circuits "Stable State" with zero output. The current flowing into the saturated base terminal of TR2 will therefore be equal to $Ib = (Vcc - 0.7)/R_T$.

If a negative trigger pulse is now applied at the input, the fast decaying edge of the pulse will pass straight through capacitor, C1 to the base of transistor, TR1 via the blocking diode turning it "ON". The collector of TR1 which was previously at Vcc drops quickly to below zero volts effectively giving capacitor C_T a reverse charge of -0.7v across its plates. This action results in transistor TR2 now having a minus base voltage at point X holding the transistor fully "OFF". This then represents the circuits second state, the "Unstable State" with an output voltage equal to Vcc.

Timing capacitor, C_T begins to discharge this -0.7v through the timing resistor R_T, attempting to charge up to the supply voltage Vcc. This negative voltage at the base of transistor TR2 begins to decrease gradually at a rate determined by the time constant of the R_T C_T combination. As the base voltage of TR2 increases back up to Vcc, the transistor begins to conduct and doing so turns "OFF" again transistor TR1 which results in the monostable multivibrator automatically returning back to its original stable state awaiting a second negative trigger pulse to restart the process once again.

Monostable Multivibrators can produce a very short pulse or a much longer rectangular shaped waveform whose leading edge rises in time with the externally applied trigger pulse and whose trailing edge is dependent upon the RC time constant of the feedback components used. This RC time constant may be varied with time to produce a series of pulses which have a controlled fixed time delay in relation to the original trigger pulse as shown below.

Monostable Multivibrator Waveforms



The time constant of **Monostable Multivibrators** can be changed by varying the values of the capacitor, C_T the resistor, R_T or both. Monostable multivibrators are generally used to increase the width of a pulse or to produce a time delay within a circuit as the frequency of the output signal is always the same as that for the trigger pulse input, the only difference is the pulse width.

This then gives us an equation for the time period of the circuit as:

$$\tau = 0.7RC$$

Where, R is in Ω and C in Farads.

MODULE 6

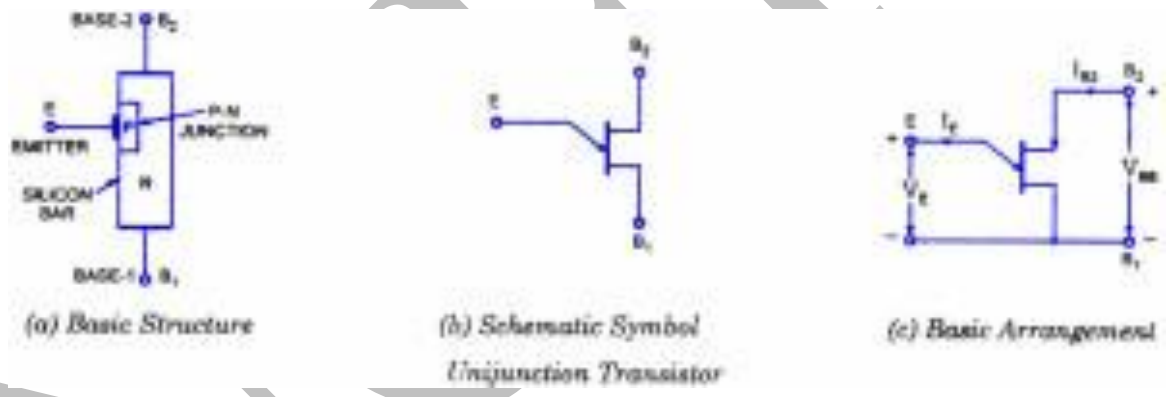
UJT, IC 555 & PLL

UJT (Uni Junction Transistor)

Uni-junction transistor is also known as double-base diode because it is a 2-layered, 3-terminal solid-state switching device. It has only one junction so it is called as a uni-junction device. The unique characteristic feature of this device is such that when it is triggered, the emitter current increases until it is restricted by an emitter power supply. Owing to its low cost, it can be used in a wide range of applications including oscillators, pulse generators and trigger circuits, etc. It is a low-power absorbing device and can be operated under normal conditions.

Construction of UJT

UJT is a three-terminal, single-junction, two-layered device, and it is similar to a thyristor compare to a transistors. It has a high-impedance off state and low-impedance on state quite similar to a thyristor. From off state to an on state, switching is caused by conductivity modulation and not by a bipolar transistor action.



(a) Basic Structure (b) Schematic Symbol (c) Basic Arrangement

Unijunction Transistor

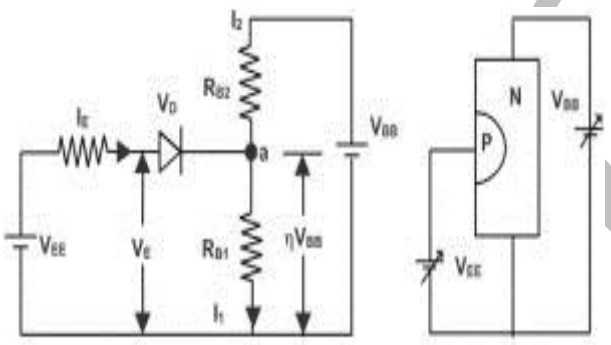
The silicon bar has two Ohmic contacts designated as base1 and base2, as shown in the fig. The function of the base and the emitter are different from the base and emitter of a bipolar transistor.

The emitter is of P-type, and it is heavily doped. The resistance between B1 and B2 when the emitter is open-circuited is called an inter-base resistance. The emitter junction is usually situated closer to the base B2 than the base B1. So the device is not symmetrical, because symmetrical unit does not provide electrical characteristics to most of the applications.

The symbol for uni-junction transistor is shown in the fig. When the device is forward-biased, it is active or is in the conducting state. The emitter is drawn at an angle to the vertical line which represents the N-type material slab and the arrow head points in the direction of conventional current.

Operation of a UJT

This transistor operation starts by making the emitter supply voltage to zero, and its emitter diode is reverse biased with the intrinsic stand-off voltage. If VB is the voltage of the emitter diode, then the total reverse bias voltage is VA + VB = Ƞ VBB + VB. For silicon VB = 0.7 V, If VE gets slowly increases to the point where VE = Ƞ VBB, then IE will be reduced to zero. Therefore, on each side of the diode, equal voltages results no current flow through it, neither in reverse bias nor in forward bias.



Equivalent Circuit of a UJT

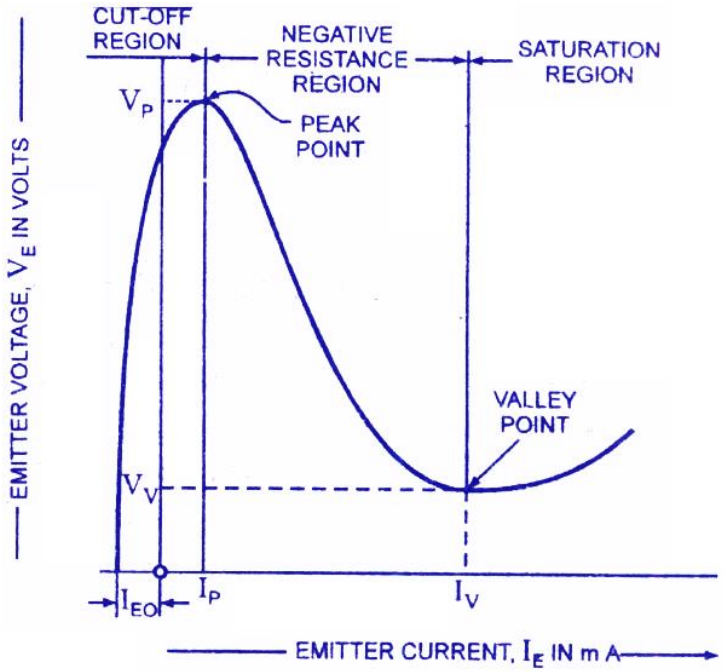
When the emitter supply voltage is increased rapidly, then the diode becomes forward-biased and exceeds the total reverse bias voltage (Ƞ VBB + VB). This emitter voltage value VE is called the peak-point voltage and is denoted by VP. When VE = VP, emitter current IE flows through the RB1 to the ground, that is, B1. This is the minimum current required for triggering the UJT. This is called the peak-point emitter current and is denoted by IP. Ip is inversely proportional to the Inter-base voltage, VBB.

Now when the emitter diode starts conducting, charge carriers are injected into the RB region of the bar. As the resistance of a semiconductor material depends upon doping, the resistance of RB decreases due to additional charge carriers.

Then the voltage drop across RB also decreases, with the decrease in resistance because the emitter diode is heavily forward biased. This in turn results in larger forward current, and as a result charge carriers are injected and it will cause the reduction in the resistance of the RB region. Thus, the emitter current goes on increasing until the emitter power supply is in limited range.

VA decreases with the increase in emitter current, and UJT have the negative resistance characteristic. The base 2 is used for applying external voltage VBB across it. The terminals E and B1 are the active terminals. UJT usually gets triggered by applying a positive pulse to the emitter, and it can be turned off by applying a negative trigger pulse.

UJT Characteristics



Static Emitter-Characteristic For a UJT

The static emitter characteristic (a curve showing the relation between emitter voltage V_E and emitter current I_E) of a **UJT** at a given inter base voltage V_{BB} is shown in figure. From figure it is noted that for emitter potentials to the left of peak point, emitter current I_E never exceeds I_{Eo} . The current I_{Eo} corresponds very closely to the reverse leakage current I_{Co} of the conventional BJT. This region, as shown in the figure, is called the cut-off region. Once conduction is established at $V_E = V_P$ the emitter potential V_E starts decreasing with the increase in emitter current I_E. This Corresponds exactly with the decrease in resistance R_B for increasing current I_E. This device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in the areas of applications listed earlier. Eventually, the valley point reaches, and any further increase in emitter current I_E places the device in the saturation region, as shown in the figure. Three other important parameters for the UJT are I_P, V_V and I_V and are defined below:

Peak-Point Emitter Current. I_p. It is the emitter current at the peak point. It represents the rnimrnum current that is required to trigger the device (UJT). It is inversely proportional to the interbase voltage V_{BB}.

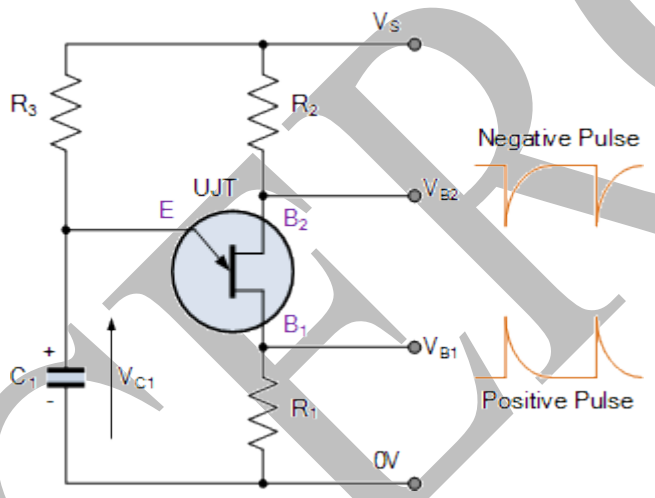
Valley Point Voltage V_V The valley point voltage is the emitter voltage at the valley point. The valley voltage increases with the increase in interbase voltage V_{BB}.

Valley Point Current I_V The valley point current is the emitter current at the valley point. It increases with the increase in inter-base voltage V_{BB}.

Special Features of UJT. The special features of a UJT are :

1. A stable triggering voltage (V_P)— a fixed fraction of applied inter base voltage V_{BB}.
2. A very low value of triggering current.
3. A high pulse current capability.
4. A negative resistance characteristic.
5. Low cost.

Uni junction Transistor Relaxation Oscillator

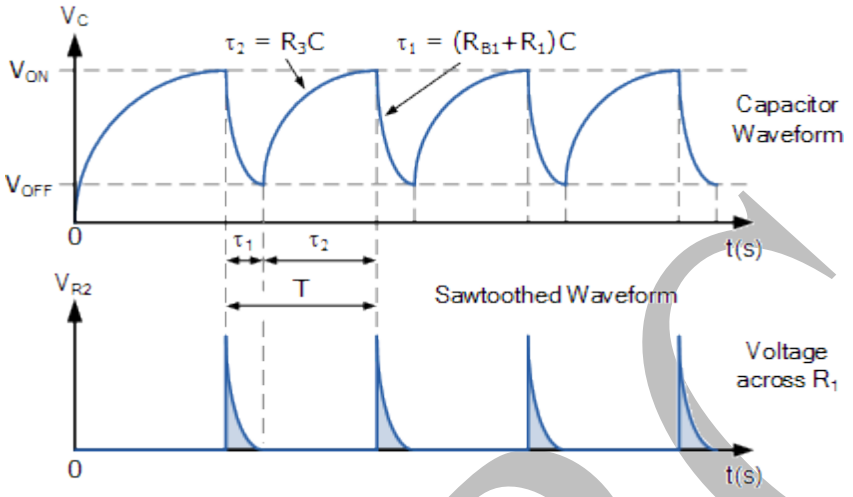


When a voltage (Vs) is firstly applied, the unijunction transistor is "OFF" and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3. As the Emitter of the UJT is connected to the capacitor, when the charging voltage Vc across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The unijunction transistor is "ON". At this point the Emitter to B1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R1 taking place.

As the ohmic value of resistor R1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R1. Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R3, the discharging time is a lot less than the charging time as the capacitor discharges through the low resistance UJT.

When the voltage across the capacitor decreases below the holding point of the p-n junction (V_{OFF}), the UJT turns "OFF" and no current flows into the Emitter junction so once again the capacitor charges up through resistor R3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, Vs applied.

UJT Oscillator Waveforms



Then we can see that the unijunction oscillator continually switches "ON" and "OFF" without any feedback. The frequency of operation of the oscillator is directly affected by the value of the charging resistance R3, in series with the capacitor C1 and the value of η. The output pulse shape generated from the Base1 (B1) terminal is that of a sawtooth waveform and to regulate the time period, you only have to change the ohmic value of resistance, R3 since it sets the RC time constant for charging the capacitor.

The time period, T of the sawtoothed waveform will be given as the charging time plus the discharging time of the capacitor. As the discharge time, τ_1 is generally very short in comparison to the larger RC charging time, τ_2 the time period of oscillation is more or less equivalent to $T \cong \tau_2$. The frequency of oscillation is therefore given by $f = 1/T$.

Uninterruptible Power Supply (UPS)

The Uninterruptible Power Supply (UPS) is an electronics device which supplies power to a load when main supplies or input power source fails. It not only acts as an emergency power source for the appliances, it serves to resolve common power problems too. Any UPS has a power storage element which stores energy in the form of chemical energy like the energy is stored in batteries.

It is like energy is stored in the form of motion in a flywheel. That is why these devices are also called battery backup or flywheel backup. The UPS not only provides emergency power, they also help to sort out common power related issues like providing protection from input power interruptions, protection from overvoltage, output voltage regulation and stabilization.

Different UPS models have different ability to supply power to the load. The degree of ability totally depends on the how much charge is stored inside the UPS. For example, the UPS designed for computers can supply power only for some small duration of time when the power goes off but that time is sufficient enough to save files on which the user may be working. So, for obvious reasons, the charge storage ability of any UPS is determined during its design considering its application.

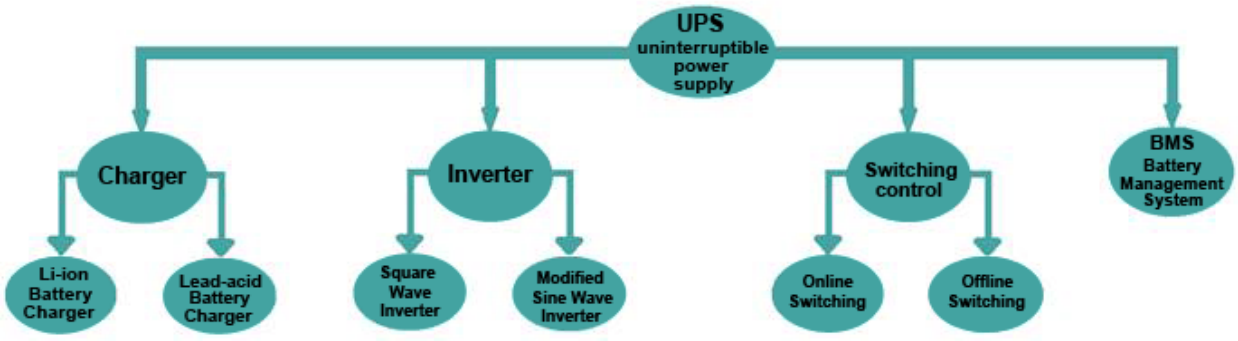


Fig. 2: Image showing Building Blocks of a UPS circuit

In this series, a UPS will be designed which will have a battery as storing element and can supply power to the appliance in case of power failure. The design of a UPS can be broken down into different sections having a distinct role in the functioning of the UPS.

i) Offline switching/standby UPS

In this type of UPS system, the load is directly connected to the mains AC supply. Whenever the AC mains voltage drops down or there is a power shut down then through a switching mechanism the load as well the battery switches to the inverter. This inverter then provides AC to the load and when power resumes, the load again switches back to the mains supply. This switching mechanism can be understood graphically from the figure below –

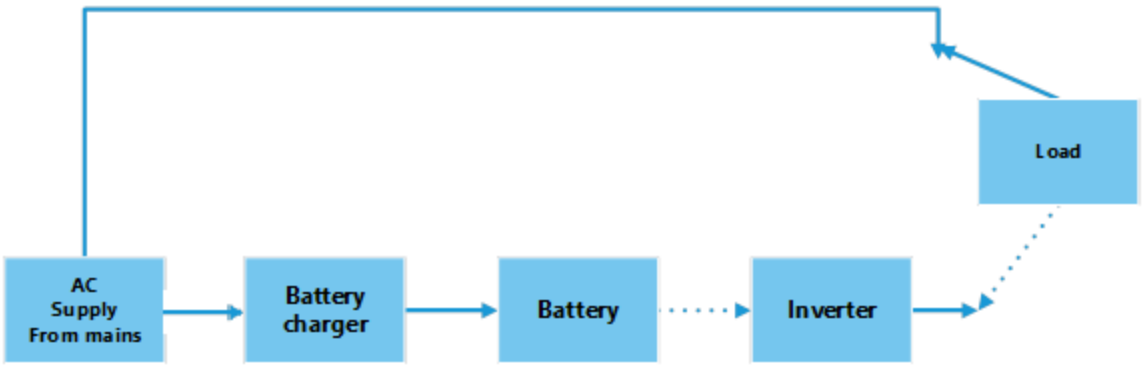


Fig. 7: Block Diagram of an Offline UPS

ii) Online switching/Double-conversion UPS

In this design, the load is always connected to the inverter. The inverter gets DC supply from the battery which is continuously charging via a battery charger. So when mains power fails the charge accumulated in the battery delivers continuous power to the appliance without any interruption.

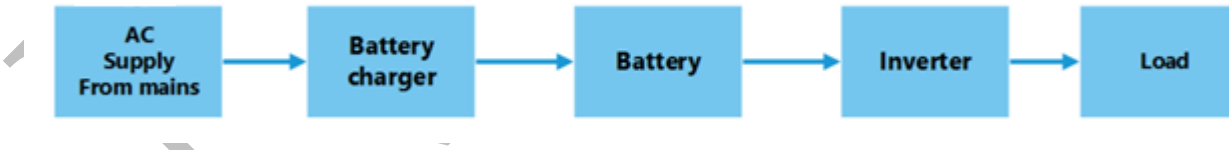


Fig. 8: Block Diagram of Online UPS

IC 555 Timer

The 555 Timer is a commonly used IC designed to produce a variety of output waveforms with the addition of an external RC network

We have seen that Multivibrators and CMOS Oscillators can be easily constructed from discrete components to produce relaxation oscillators for generating basic square wave output waveforms. But there are also dedicated IC's especially designed to accurately produce the required output waveform with the addition of just a few extra timing components.

One such device that has been around since the early days of IC's and has itself become something of an industry "standard" is the **555 Timer Oscillator** which is more commonly called the **"555 Timer"**.

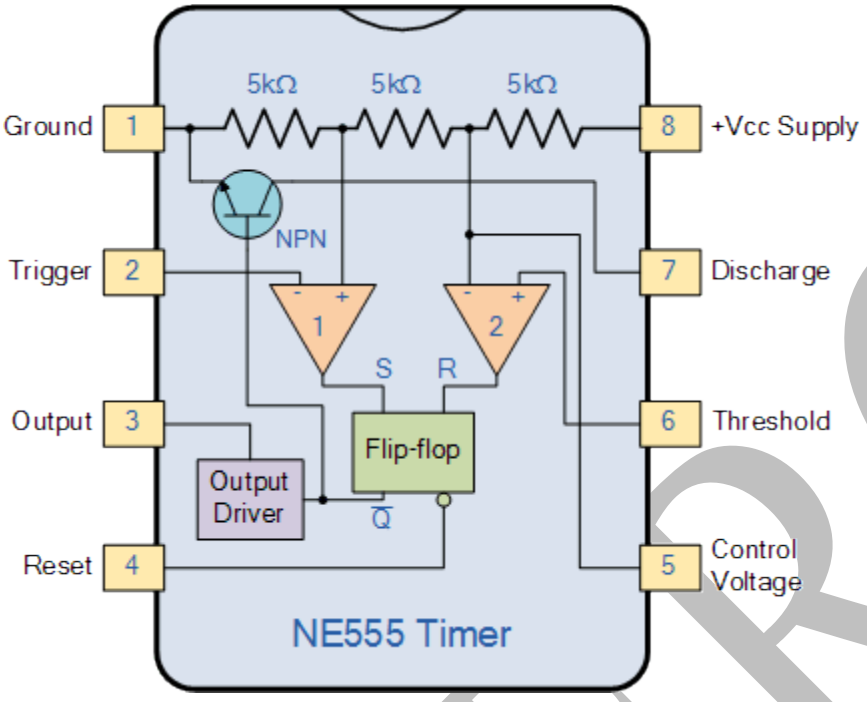
The basic **555 timer** gets its name from the fact that there are three internally connected 5kΩ resistors which it uses to generate the two comparators reference voltages. The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilised waveforms of varying duty cycles from 50 to 100%.

The 555 timer chip is extremely robust and stable 8-pin device that can be operated either as a very accurate Monostable, Bistable or Astable Multivibrator to produce a variety of applications such as one-shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc, in fact any circuit that requires some form of time control as the list is endless.

The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip-flop and a high current output stage as shown below. As well as the 555 Timer there is also available the NE556 Timer Oscillator which combines TWO individual 555's within a single 14-pin DIP package and low power CMOS versions of the single 555 timer such as the 7555 and LMC555 which use MOSFET transistors instead.

A simplified "block diagram" representing the internal circuitry of the **555 timer** is given below with a brief explanation of each of its connecting pins to help provide a clearer understanding of how it works.

555 Timer Block Diagram



- • Pin 1. – **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.
- • Pin 2. – **Trigger**, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.
- • Pin 3. – **Output**, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc – 1.5V so small speakers, LEDs or motors can be connected directly to the output.
- • Pin 4. – **Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.
- • Pin 5. – **Control Voltage**, This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.
- • Pin 6. – **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from "HIGH" to "LOW" state. This pin connects directly to the RC timing circuit.

- • Pin 7. – **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "LOW".
- • Pin 8. – **Supply +Vcc**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

The **555 Timers** name comes from the fact that there are three 5kΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the negative inverting input of comparator two at 2/3Vcc and the positive non-inverting input to comparator one at 1/3Vcc.

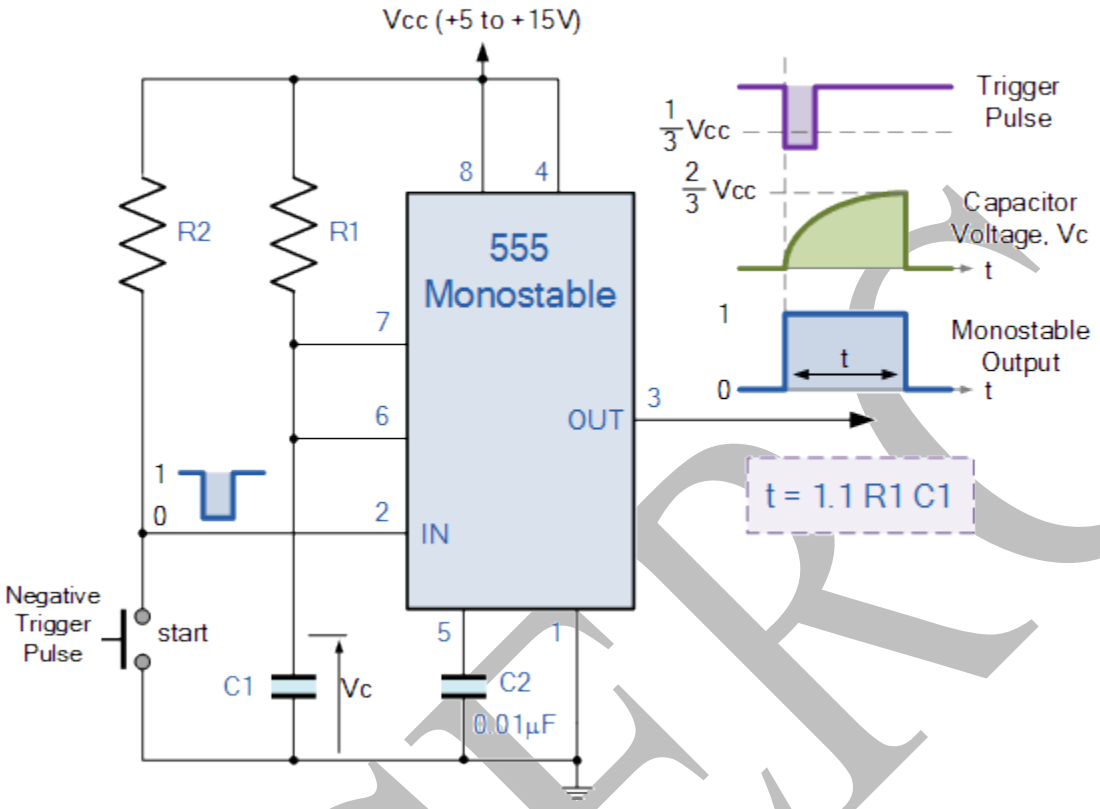
The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a "HIGH" or "LOW" level output at Q based on the states of its inputs. The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a "HIGH" or "LOW" voltage level at the output pin.

The most common use of the 555 timer oscillator is as a simple astable oscillator by connecting two resistors and a capacitor across its terminals to generate a fixed pulse train with a time period determined by the time constant of the RC network. But the 555 timer oscillator chip can also be connected in a variety of different ways to produce Monostable or Bistable multivibrators as well as the more common Astable Multivibrator.

The Monostable 555 Timer

The operation and output of the **555 timer monostable** is exactly the same as that for the transistorised one we look at previously in the Monostable Multivibrators tutorial. The difference this time is that the two transistors have been replaced by the 555 timer device. Consider the 555 timer monostable circuit below.

Monostable 555 Timer



When a negative (0V) pulse is applied to the trigger input (pin 2) of the Monostable configured 555 Timer oscillator, the internal comparator, (comparator No1) detects this input and "sets" the state of the flip-flop, changing the output from a "LOW" state to a "HIGH" state. This action in turn turns "OFF" the discharge transistor connected to pin 7, thereby removing the short circuit across the external timing capacitor, C1.

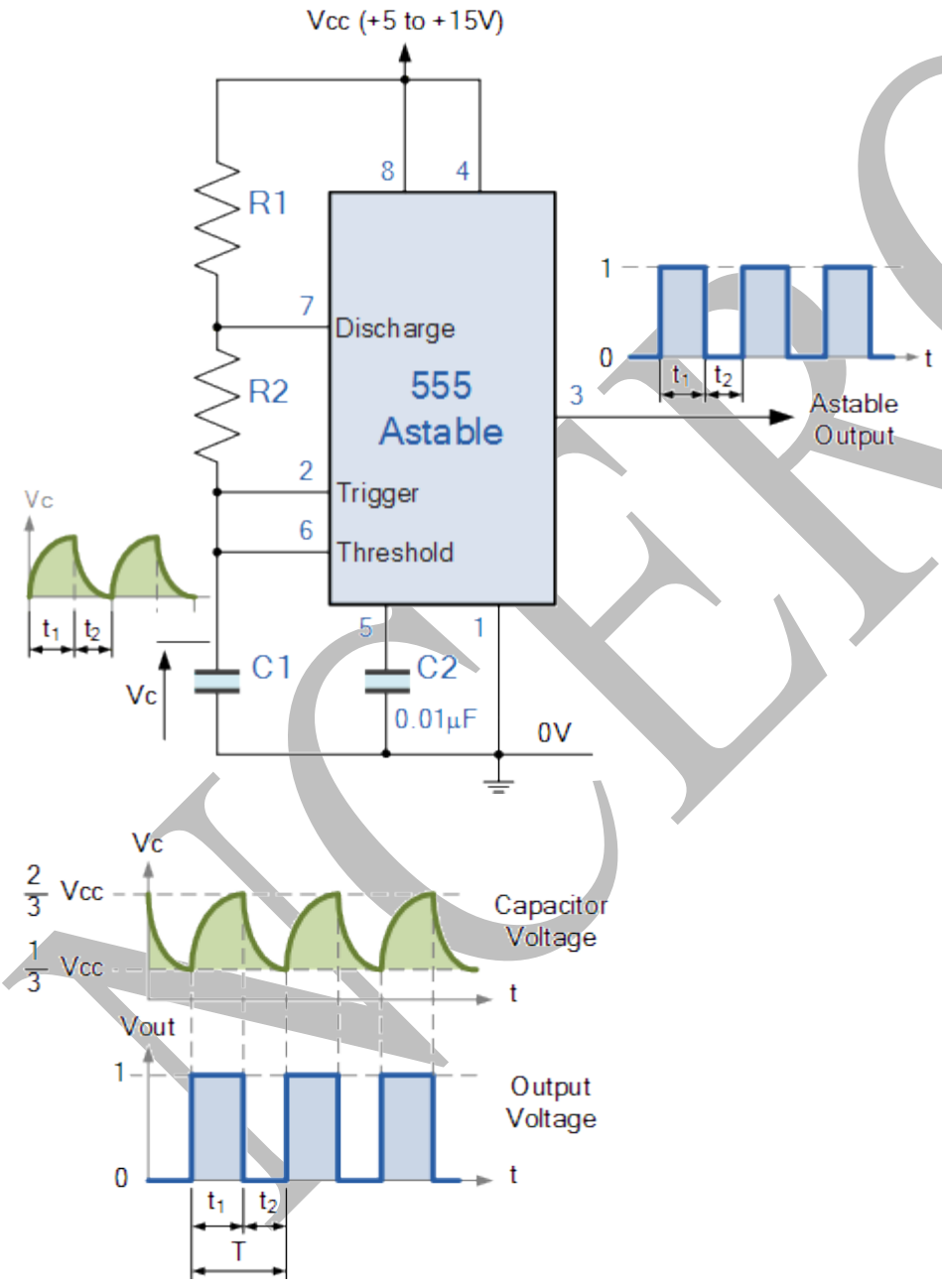
This action allows the timing capacitor to start to charge up through resistor, R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of 2/3Vcc set up by the internal voltage divider network. At this point the comparators output goes "HIGH" and "resets" the flip-flop back to its original state which in turn turns "ON" the transistor and discharges the capacitor to ground through pin 7. This causes the output to change its state back to the original stable "LOW" value awaiting another trigger pulse to start the timing process over again. Then as before, the Monostable Multivibrator has only "ONE" stable state.

The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this "HIGH" unstable output state until the time period set up by the R_1 x C_1 network has elapsed. The amount of time that the output voltage remains "HIGH" or at a logic "1" level, is given by the following time constant equation.

$$\tau = 1.1 R_1 C_1$$

Where, t is in seconds, R is in Ω and C in Farads.

Astable 555 Oscillator Circuit



In the **555 Oscillator** circuit above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the *discharge* terminal, pin 7.

Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the 0.693(R1+R2)C combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the 0.693(R2*C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc – 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required to complete one charge and discharge cycle of the output is therefore given as:

Astable 555 Oscillator Charge and Discharge Times

$$t_1 = 0.693(R_1 + R_2).C$$

and

$$t_2 = 0.693 \times R_2 \times C$$

Where, R is in Ω and C in Farads.

When connected as an astable multivibrator, the output from the **555 Oscillator** will continue indefinitely charging and discharging between 2/3Vcc and 1/3Vcc until the power supply is removed. As with the monostable multivibrator these charge and discharge times and therefore the frequency are independent on the supply voltage.

The duration of one full timing cycle is therefore equal to the sum of the two individual times that the capacitor charges and discharges added together and is given as:

555 Oscillator Cycle Time

$$T = t_1 + t_2 = 0.693(R_1 + 2R_2).C$$

The output frequency of oscillations can be found by inverting the equation above for the total cycle time giving a final equation for the output frequency of an Astable 555 Oscillator as:

555 Oscillator Frequency Equation

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2).C}$$

By altering the time constant of just one of the RC combinations, the **Duty Cycle** better known as the "Mark-to-Space" ratio of the output waveform can be accurately set and is given as the ratio of resistor R2 to resistor R1. The Duty Cycle for the 555 Oscillator, which is the ratio of the "ON" time divided by the "OFF" time is given by:

555 Oscillator Duty Cycle

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$

The duty cycle has no units as it is a ratio but can be expressed as a percentage (%). If both timing resistors, R1 and R2 are equal in value, then the output duty cycle will be 2:1 that is, 66% ON time and 33% OFF time with respect to the period.

PHASE LOCKED LOOPS(PLL)

Phase Locked Loop **(PLL)** is one of the vital blocks in linear systems. It is useful in communication systems such as radars, satellites, FMs, etc.

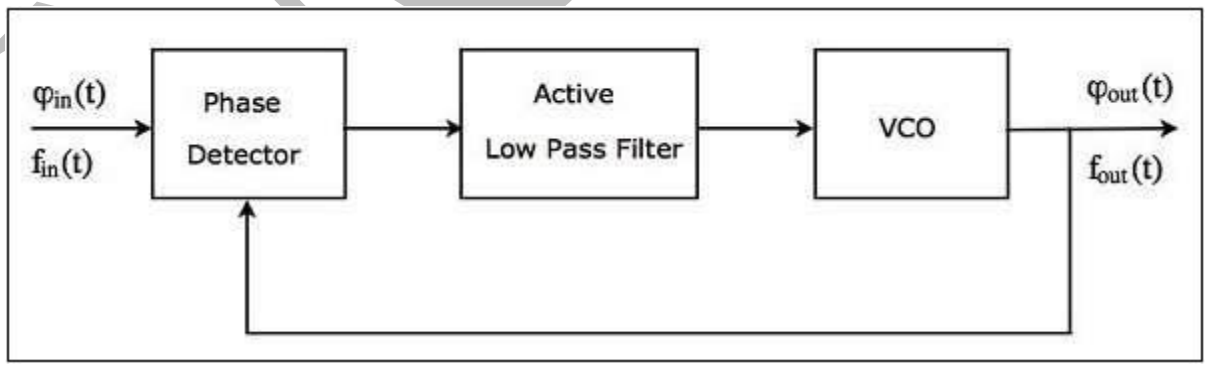
This chapter discusses about the block diagram of PLL and IC 565 in detail.

Block Diagram of PLL

A Phase Locked Loop (PLL) mainly consists of the following **three blocks** −

- Phase Detector
- Active Low Pass Filter
- Voltage Controlled Oscillator (VCO)

The **block diagram** of PLL is shown in the following figure −



The output of a phase detector is applied as an input of active low pass filter. Similarly, the output of active low pass filter is applied as an input of VCO.

The **working** of a PLL is as follows −

- **Phase detector** produces a DC voltage, which is proportional to the phase difference between the input signal having frequency of fin and feedback (output) signal having frequency of fout.
- A **Phase detector** is a multiplier and it produces two frequency components at its output − sum of the frequencies fin and fout and difference of frequencies fin & fout.
- An **active low pass filter** produces a DC voltage at its output, after eliminating high frequency component present in the output of the phase detector. It also amplifies the signal.
- A **VCO** produces a signal having a certain frequency, when there is no input applied to it. This frequency can be shifted to either side by applying a DC voltage to it. Therefore, the frequency deviation is directly proportional to the DC voltage present at the output of a low pass filter.

The above operations take place until the VCO frequency equals to the input signal frequency. Based on the type of application, we can use either the output of active low pass filter or output of a VCO. PLLs are used in many **applications** such as FM demodulator, clock generator etc.

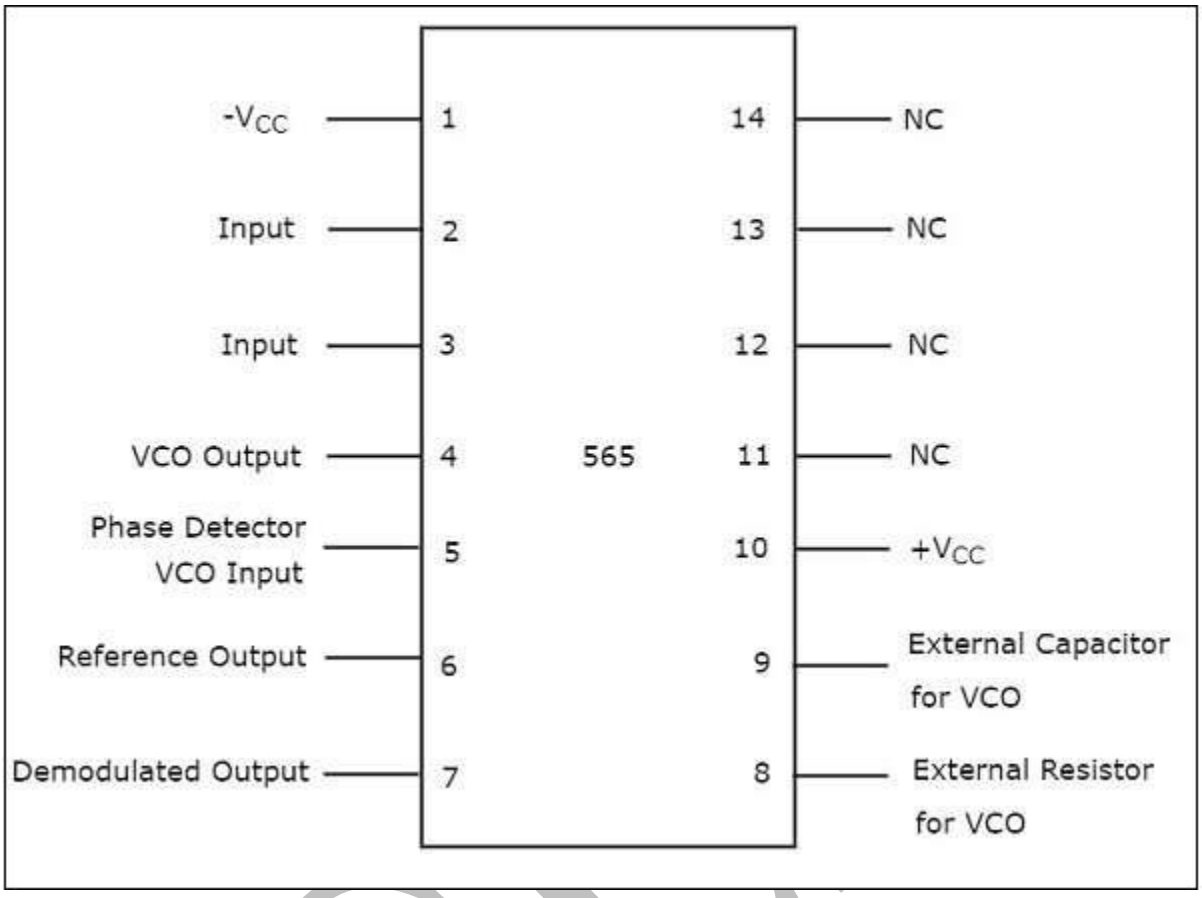
PLL operates in one of the **following three modes** −

- Free running mode
- Capture mode
- Lock mode

Initially, PLL operates in **free running mode** when no input is applied to it. When an input signal having some frequency is applied to PLL, then the output signal frequency of VCO will start change. At this stage, the PLL is said to be operating in the **capture mode**. The output signal frequency of VCO will change continuously until it is equal to the input signal frequency. Now, it is said to be PLL is operating in the **lock mode**.

IC 565

IC 565 is the most commonly used phase locked loop IC. It is a 14 pin Dual-Inline Package (DIP). The **pin diagram** of IC 565 is shown in the following figure −



The purpose of each pin is self-explanatory from the above diagram. Out of 14 pins, only 10 pins (pin number 1 to 10) are utilized for the operation of PLL. So, the remaining 4 pins (pin number 11 to 14) are labelled with NC (No Connection).

The **VCO** produces an output at pin number 4 of IC 565, when the pin numbers 2 and 3 are grounded. Mathematically, we can write the output frequency, fout of the VCO as.

$$fout=0.25RvCvfout=0.25RVCV$$

where,

Rv is the external resistor that is connected to the pin number 8

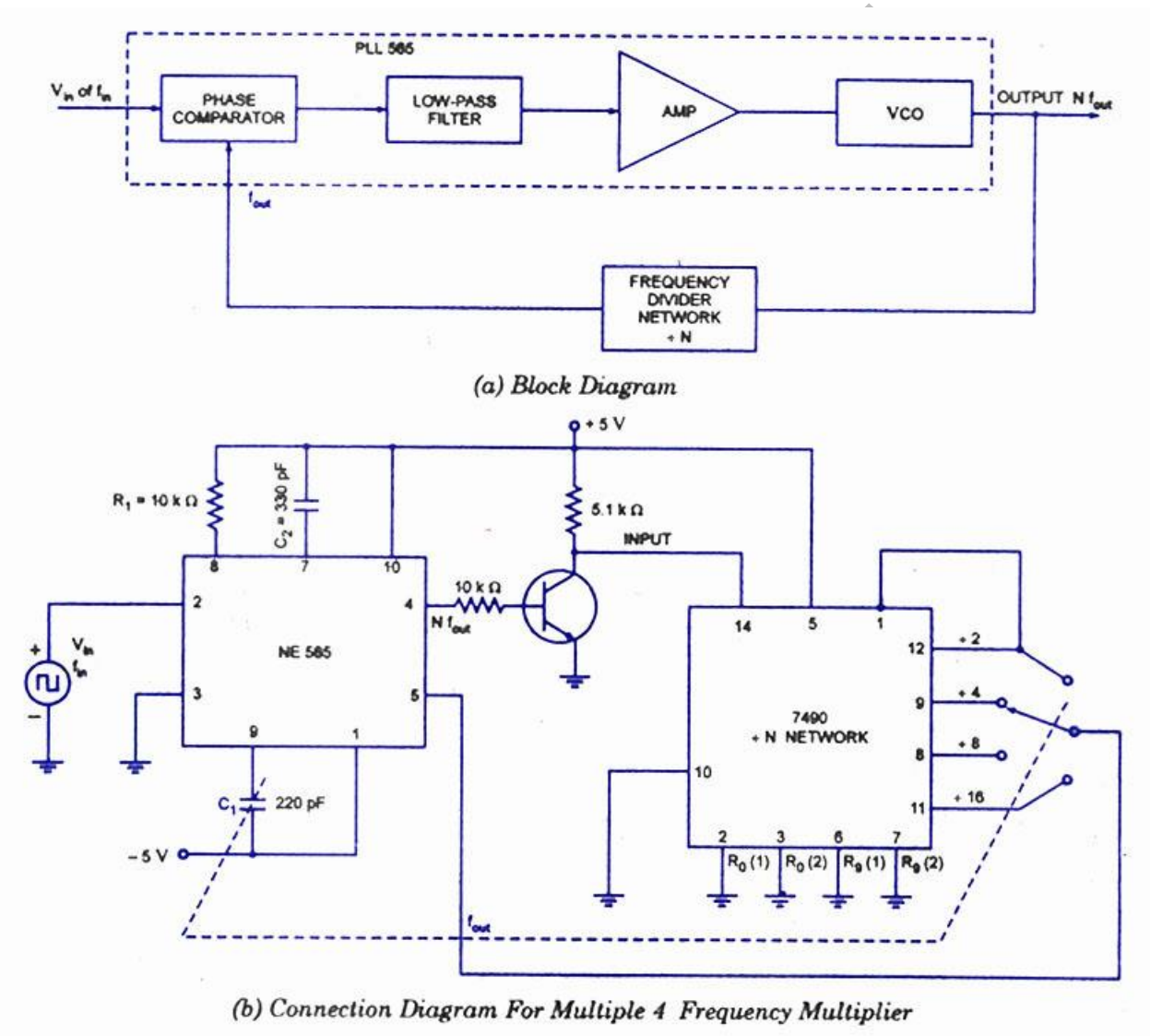
Cv is the external capacitor that is connected to the pin number 9

- By choosing proper values of Rv and Cv, we can fix (determine) the output frequency, fout of VCO.
- **Pin numbers 4 and 5**are to be shorted with an external wire so that the output of VCO can be applied as one of the inputs of phase detector.

- IC 565 has an internal resistance of 3.6KΩ. A capacitor, C has to be connected between pin numbers 7 and 10 in order to make a **low pass filter** with that internal resistance.

Note that as per the requirement, we have to properly configure the pins of IC 565.

Frequency Multiplication or Frequency Synthesis Using PLL



The block diagram of a frequency muliplier (or synthesizer) is shown in figure. In this circuit, a frequency divider is inserted between the output of the VCO and the phase comparator (PC) so that the loop signal to the PC is at frequency f_{OUT} while the output of VCO is N f_{OUT}. This output is a multiple of the input frequency as long as the loop is in lock. The desired amount of multiplication can be obtained by selecting a proper divide- by N network where N is an integer. Figure shows this function performed by a 7490 configured as a divide-by-4 circuit.

In this case the input V_{in} at frequency $/_{in}$ is compared with the output frequency f_{OUT} at pin 5. An output at N f_{OUT} (4 f_{OUT} in this case) is connected through an inverter circuit to give an input at pin 14 of the 7490, which varies between 0 and + 5 V. Using the output at pin 9, which is one-fourth of that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock.

Since the VCO can be adjusted over a limited range from its centre frequency, it may become necessary to change the VCO frequency whenever the divider value is changed.

CONTENT BEYOND SYLLABUS

WIEN BRIDGE OSCILLATOR

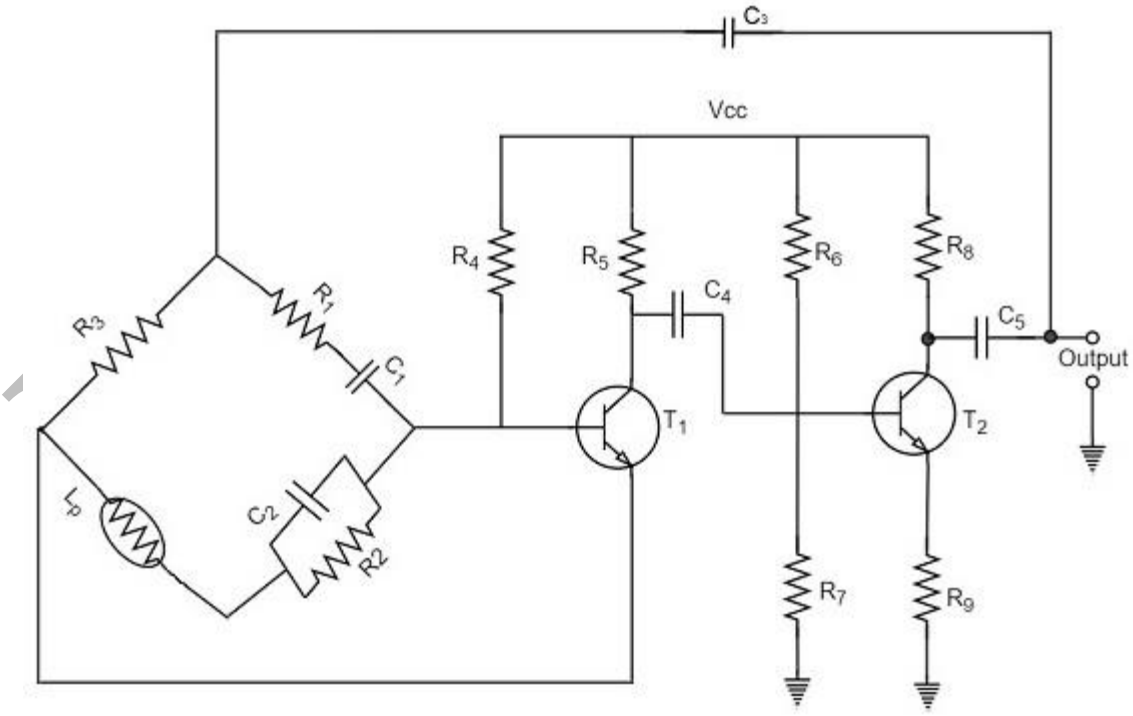
Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the **circuit fluctuations** and the **ambient temperature**.

The main advantage of this oscillator is that the frequency can be varied in the range of 10Hz to about 1MHz whereas in RC oscillators, the frequency is not varied.

Construction

The circuit construction of Wien bridge oscillator can be explained as below. It is a two-stage amplifier with RC bridge circuit. The bridge circuit has the arms R_1C_1, R_3, R_2C_2 and the tungsten lamp L_p. Resistance R_3 and the lamp L_p are used to stabilize the amplitude of the output.

The following circuit diagram shows the arrangement of a Wien bridge oscillator.



The transistor T_1 serves as an oscillator and an amplifier while the other transistor T_2 serves as an inverter. The inverter operation provides a phase shift of 180^o. This circuit provides positive

feedback through R_1C_1, C_2R_2 to the transistor T_1 and negative feedback through the voltage divider to the input of transistor T_2.

The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

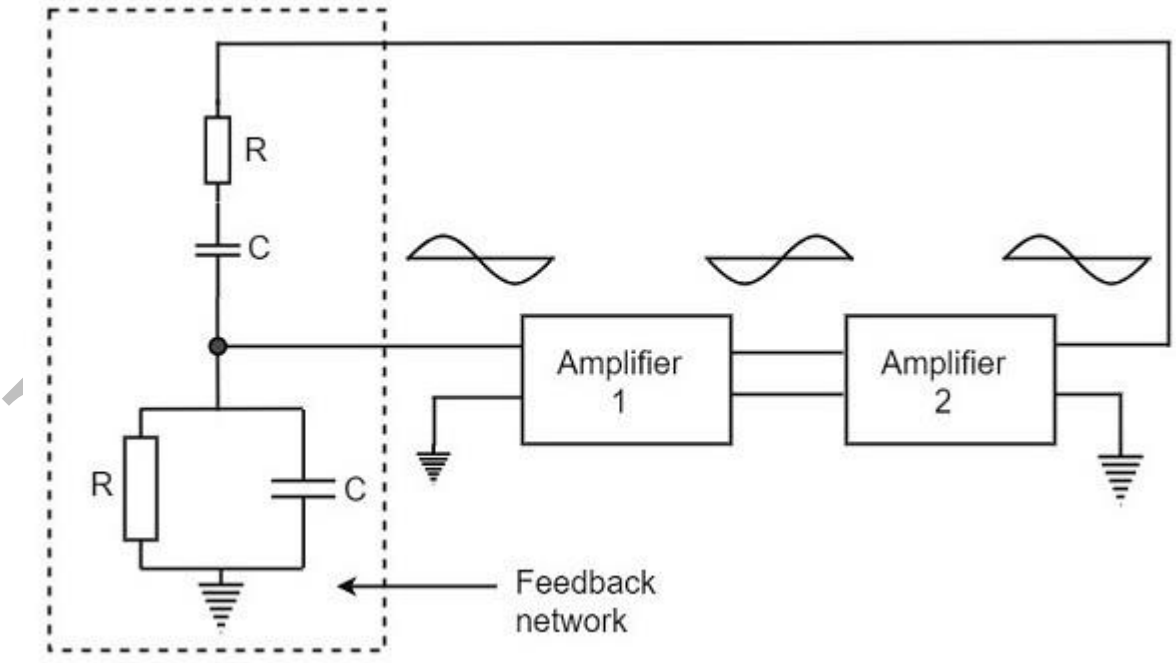
$$f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If $R_1 = R_2$ and $C_1 = C_2 = C$

Then,

$$f = \frac{1}{2\pi RC}$$

Now, we can simplify the above circuit as follows −



The oscillator consists of two stages of RC coupled amplifier and a feedback network. The voltage across the parallel combination of R and C is fed to the input of amplifier 1. The net phase shift through the two amplifiers is zero.

The usual idea of connecting the output of amplifier 2 to amplifier 1 to provide signal regeneration for oscillator is not applicable here as the amplifier 1 will amplify signals over a wide range of frequencies and hence direct coupling would result in poor frequency stability. By adding Wien bridge feedback network, the oscillator becomes sensitive to a particular frequency and hence frequency stability is achieved.

Operation

When the circuit is switched ON, the bridge circuit produces oscillations of the frequency stated above. The two transistors produce a total phase shift of 360^o so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by temperature sensitive tungsten lamp L_p. Its resistance increases with current.

If the amplitude of the output increases, more current is produced and more negative feedback is achieved. Due to this, the output would return to the original value. Whereas, if the output tends to decrease, reverse action would take place.

Advantages

The advantages of Wien bridge oscillator are as follows −

- The circuit provides good frequency stability.
- It provides constant output.
- The operation of circuit is quite easy.
- The overall gain is high because of two transistors.
- The frequency of oscillations can be changed easily.
- The amplitude stability of the output voltage can be maintained more accurately, by replacing R_2 with a thermistor.

Disadvantages

The disadvantages of Wien bridge oscillator are as follows −

- The circuit cannot generate very high frequencies.
- Two transistors and number of components are required for the circuit construction.

Crystal Oscillators

Whenever an oscillator is under continuous operation, its frequency stability gets affected. There occur changes in its frequency. The main factors that affect the frequency of an oscillator are

- Power supply variations
- Changes in temperature
- Changes in load or output resistance

In RC and LC oscillators the values of resistance, capacitance and inductance vary with temperature and hence the frequency gets affected. In order to avoid this problem, the piezo electric crystals are being used in oscillators.

The use of piezo electric crystals in parallel resonant circuits provide high frequency stability in oscillators. Such oscillators are called as Crystal Oscillators.

Crystal Oscillators

The principle of crystal oscillators depends upon the Piezo electric effect. The natural shape of a crystal is hexagonal. When a crystal wafer is cur perpendicular to X-axis, it is called as X-cut and when it is cut along Y-axis, it is called as Y-cut.

The crystal used in crystal oscillator exhibits a property called as Piezo electric property. So, let us have an idea on piezo electric effect.

Piezo Electric Effect

The crystal exhibits the property that when a mechanical stress is applied across one of the faces of the crystal, a potential difference is developed across the opposite faces of the crystal. Conversely, when a potential difference is applied across one of the faces, a mechanical stress is produced along the other faces. This is known as Piezo electric effect.

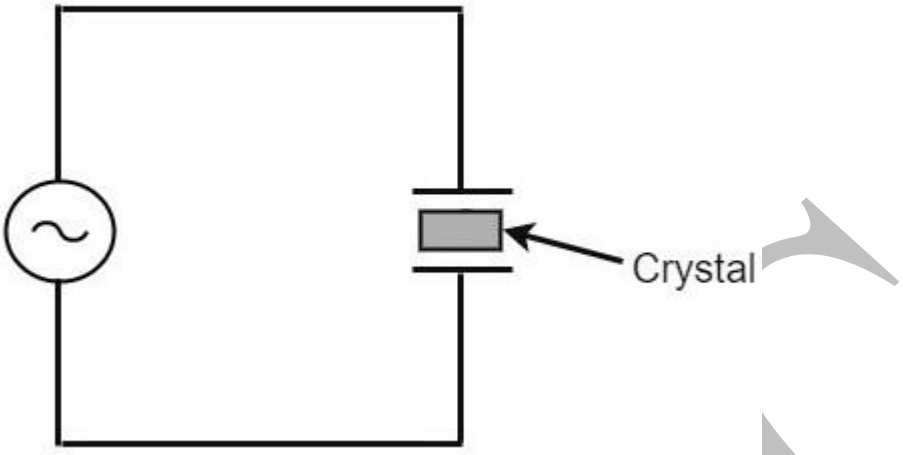
Certain crystalline materials like Rochelle salt, quartz and tourmaline exhibit piezo electric effect and such materials are called as Piezo electric crystals. Quartz is the most commonly used piezo electric crystal because it is inexpensive and readily available in nature.

When a piezo electric crystal is subjected to a proper alternating potential, it vibrates mechanically. The amplitude of mechanical vibrations becomes maximum when the frequency of alternating voltage is equal to the natural frequency of the crystal.

Working of a Quartz Crystal

In order to make a crystal work in an electronic circuit, the crystal is placed between two metal plates in the form of a capacitor. Quartz is the mostly used type of crystal because of its availability and strong nature while being inexpensive. The ac voltage is applied in parallel to the crystal.

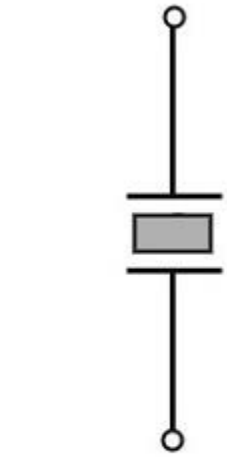
The circuit arrangement of a Quartz Crystal will be as shown below −



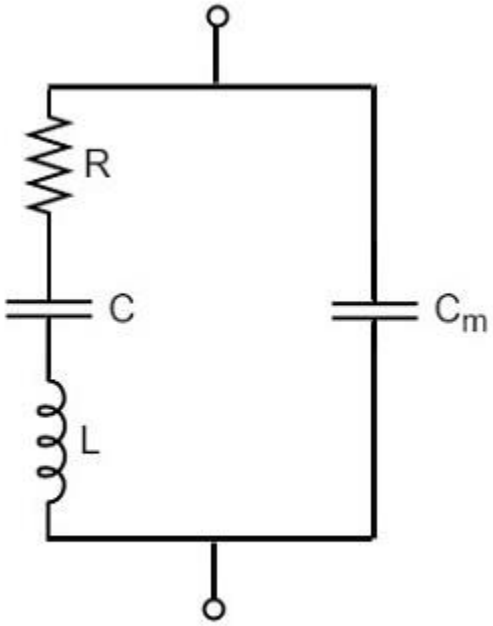
If an AC voltage is applied, the crystal starts vibrating at the frequency of the applied voltage. However, if the frequency of the applied voltage is made equal to the natural frequency of the crystal, resonance takes place and crystal vibrations reach a maximum value. This natural frequency is almost constant.

Equivalent circuit of a Crystal

If we try to represent the crystal with an equivalent electric circuit, we have to consider two cases, i.e., when it vibrates and when it doesn't. The figures below represent the symbol and electrical equivalent circuit of a crystal respectively.



Symbol of a Crystal



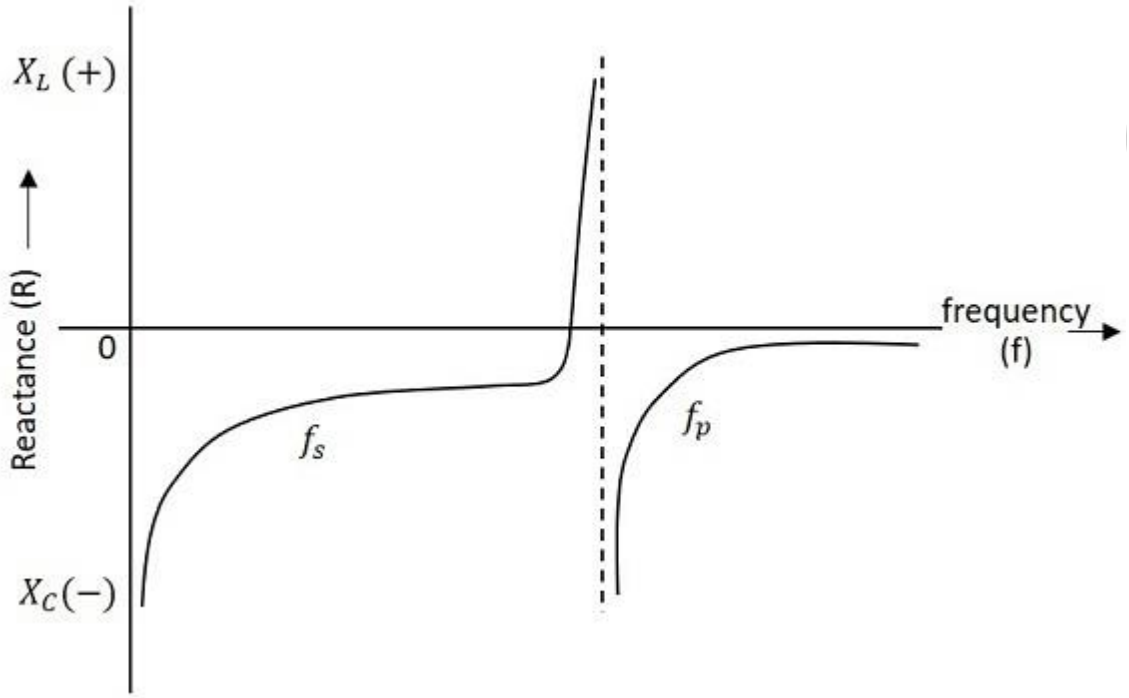
Equivalent circuit of a crystal

The above equivalent circuit consists of a series R-L-C circuit in parallel with a capacitance C_m.

When the crystal mounted across the AC source is not vibrating, it is equivalent to the capacitance C_m. When the crystal vibrates, it acts like a tuned R-L-C circuit.

Frequency response

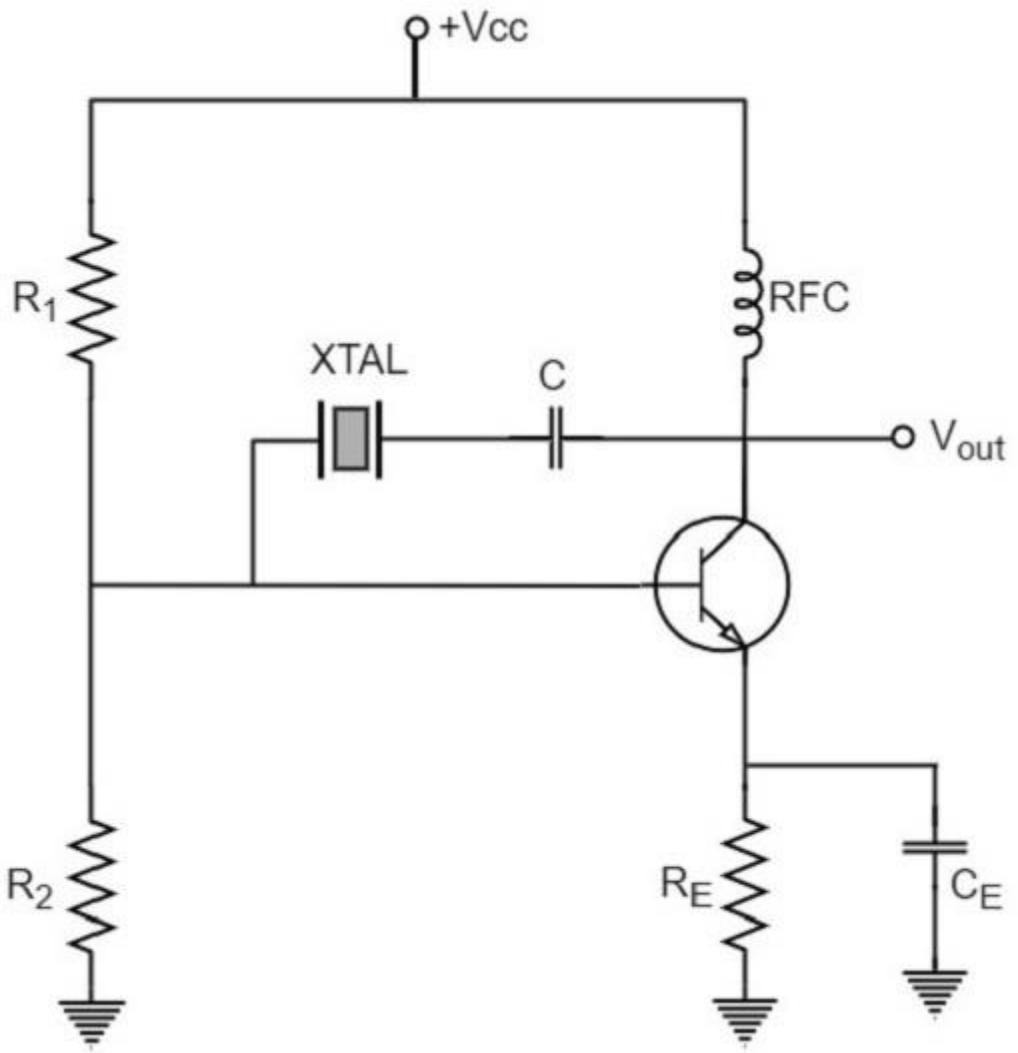
The frequency response of a crystal is as shown below. The graph shows the reactance (X_L or X_C) versus frequency (f). It is evident that the crystal has two closely spaced resonant frequencies.



Crystal Oscillator Circuit

A crystal oscillator circuit can be constructed in a number of ways like a Crystal controlled tuned collector oscillator, a Colpitts crystal oscillator, a Clap crystal oscillator etc. But the transistor pierce crystal oscillator is the most commonly used one. This is the circuit which is normally referred as a crystal oscillator circuit.

The following circuit diagram shows the arrangement of a transistor pierce crystal oscillator.



In this circuit, the crystal is connected as a series element in the feedback path from collector to the base. The resistors R_1, R_2 and R_E provide a voltage-divider stabilized d.c. bias circuit. The capacitor C_E provides a.c. bypass of the emitter resistor and RFC (radio frequency choke) coil provides for d.c. bias while decoupling any a.c. signal on the power lines from affecting the output signal. The coupling capacitor C has negligible impedance at the circuit operating frequency. But it blocks any d.c. between collector and base.

Advantages

- They have a high order of frequency stability.
- The quality factor (Q) of the crystal is very high.

Disadvantages

- They are fragile and can be used in low power circuits.
- The frequency of oscillations cannot be changed appreciably.

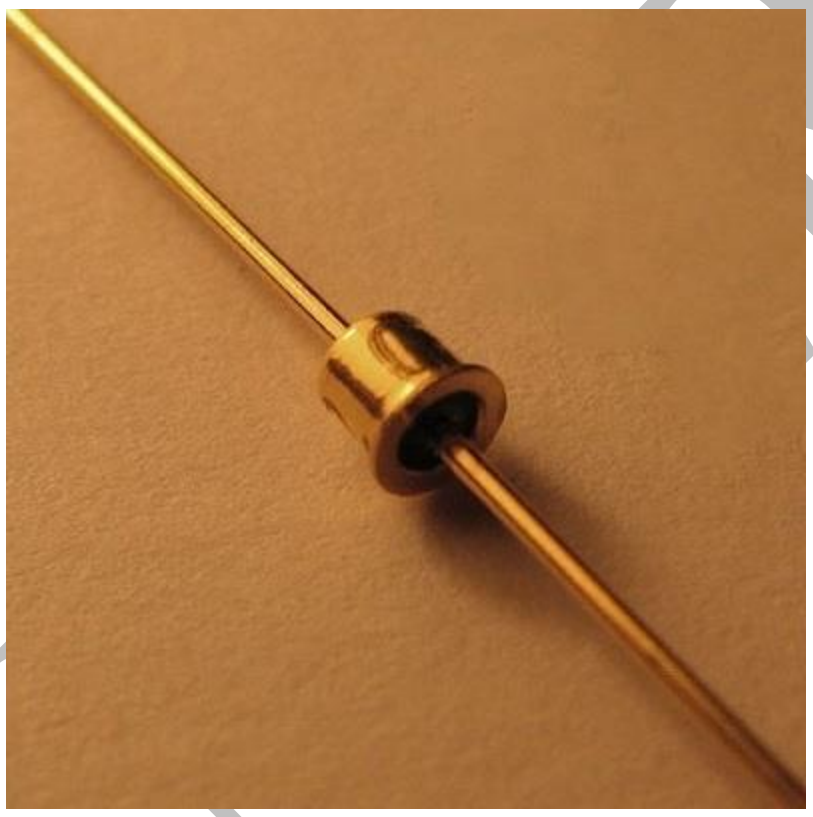
Tunnel Diode Oscillator

The oscillator circuit that is built using a tunnel diode is called as a Tunnel diode oscillator. If the impurity concentration of a normal PN junction is highly increased, this **Tunnel diode** is formed. It is also known as **Esaki diode**, after its inventor.

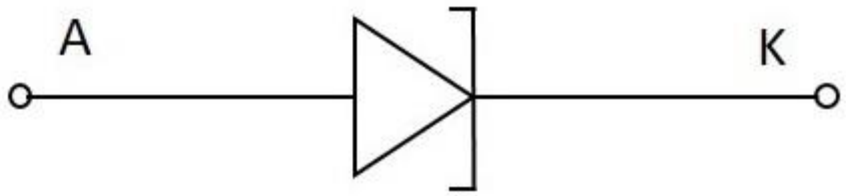
Tunnel Diode

When the impurity concentration in a diode increases, the width of depletion region decreases, extending some extra force to the charge carriers to cross the junction. When this concentration is further increased, due to less width of the depletion region and the increased energy of the charge carriers, they penetrate through the potential barrier, instead of climbing over it. This penetration can be understood as **Tunneling** and hence the name, **Tunnel diode**.

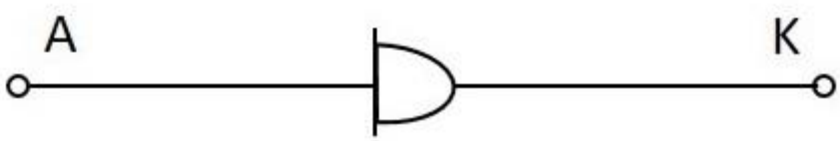
The following image shows how a practical tunnel diode looks like.



The symbols of tunnel diode are as shown below.



or



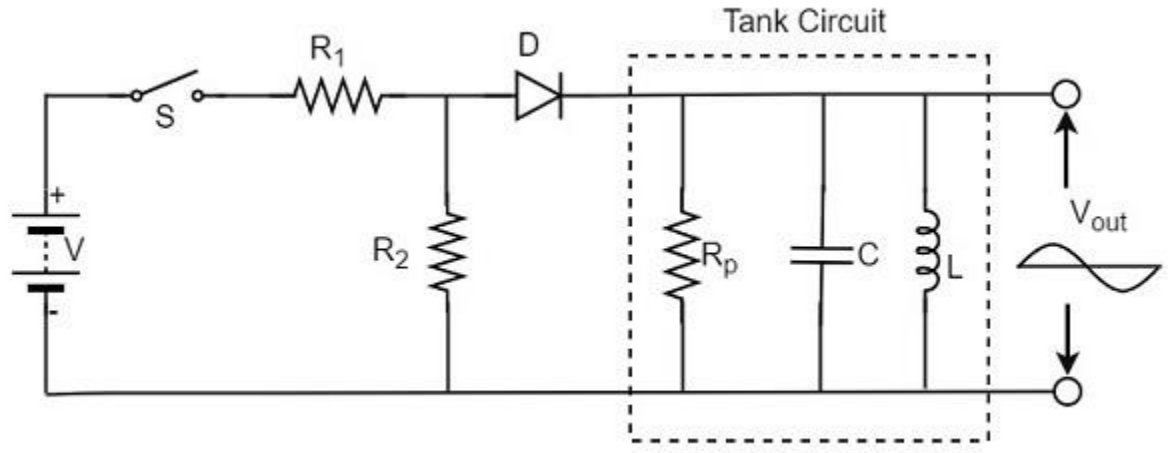
Symbol of Tunnel diode

Tunnel Diode Oscillator

The tunnel diode helps in generating a very high frequency signal of nearly 10GHz. A practical tunnel diode circuit may consist of a switch S, a resistor R and a supply source V, connected to a tank circuit through a tunnel diode D.

Working

The value of resistor selected should be in such a way that it biases the tunnel diode in the midway of the negative resistance region. The figure below shows the practical tunnel diode oscillator circuit.



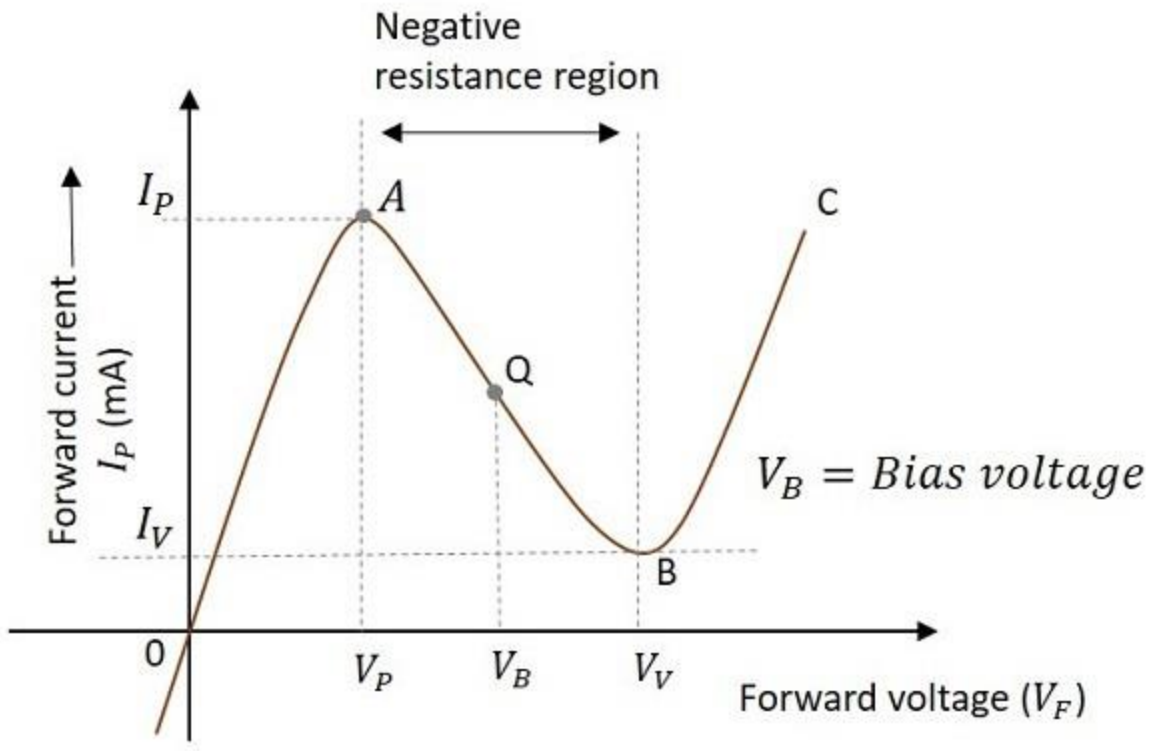
In this circuit, the resistor R_1 sets proper biasing for the diode and the resistor R_2 sets proper current level for the tank circuit. The parallel combination of resistor R_p inductor L and capacitor C form a tank circuit, which resonates at the selected frequency.

When the switch S is closed, the circuit current rises immediately towards the constant value, whose value is determined by the value of resistor R and the diode resistance. However, as the voltage drop across the tunnel diode V_D exceeds the peak-point voltage V_p, the tunnel diode is driven into negative resistance region.

In this region, the current starts decreasing, till the voltage V_D becomes equal to the valleypoint voltage V_v. At this point, a further increase in the voltage V_D drives the diode into positive resistance region. As a result of this, the circuit current tends to increase. This increase in circuit will increase the voltage drop across the resistor R which will reduce the voltage V_D.

V-I characteristic curve

The following graph shows the V-I characteristics of a tunnel diode −



The curve AB indicates the negative resistance region as the resistance decreases while the voltage increases. It is clear that the Q-point is set at the middle of the curve AB. The Q-point can move between the points A and B during the circuit operation. The point A is called **peak point** and the point B is called **valley point**.

During the operation, after reaching the point B, the increase in circuit current will increase the voltage drop across the resistor R which will reduce the voltage V_D. This brings the diode back into negative resistance region.

The decrease in voltage V_D is equal to the voltage V_P and this completes one cycle of operation. The continuation of these cycles produces continuous oscillations which give a sinusoidal output.

Advantages

The advantages of a tunnel diode oscillator are as follows −

- It has high switching speeds.
- It can handle high frequencies.

Disadvantages

The disadvantages of a tunnel diode oscillator are as follows −

- They are low power devices.
- Tunnel diodes are a bit costly.

Applications

The applications of a tunnel diode oscillator are as follows −

- It is used in relaxation oscillators.
- It is used in microwave oscillators.
- It is also used as Ultra high speed switching device.
- It is used as logic memory storage device.

After having covered all the major sinusoidal oscillator circuits, it is to be noted that there are many oscillators like the ones mentioned till now. The oscillators which produce sine waveforms are sinusoidal oscillators as discussed.

The oscillators which produce non-sinusoidal waveforms (rectangular, sweep, triangular etc.) are non-sinusoidal oscillators which we have discussed in detail in our Pulse Circuits tutorial.